SYNOOS

DATA SHEET

VLN5P Series *(OTP)*

Single-Chip 4-bit MCU with 15~24 I/O, ‘1-Ch Speech + Dual-Tone’ or ‘4-Ch Speech/Midi’

Version 1.5

Jul. 4, 2013

1. GENERAL DESCRIPTION

The VLN5P series IC is a powerful 4-bit micro-controller based sound processor. They are embedded EPROM architecture, and the OTP (One Time Programmable) ICs that are designed to support VLN5P and MaskROM products. There are 4 channels that are configured as speech, tone or midi, and all of them can be auto-played back simultaneously. By using the high fidelity ADPCM speech synthesis algorithm, it can produce outstanding quality voices. Wide range sampling rate up to 44.1kHz and different volume level are supported. It is also equipped two kinds of audio outputs with fine resolution, including a current D/A converter and a PWM direct-drive. The RISC MCU architecture is very easy to program and control, various applications can be easily implemented. There are 48 instructions, and most of them are executed in single cycle. Through +/-1% accurate internal oscillation, external Rosc is mostly unnecessary. Also an OSC pad is reserved for external oscillation, and this pad can be optioned as normal I/O when setting internal oscillation only. Furthermore, in addition to the HALT mode (sleep mode), it offers the SLOW mode to minimize power dissipation.

2. FEATURES

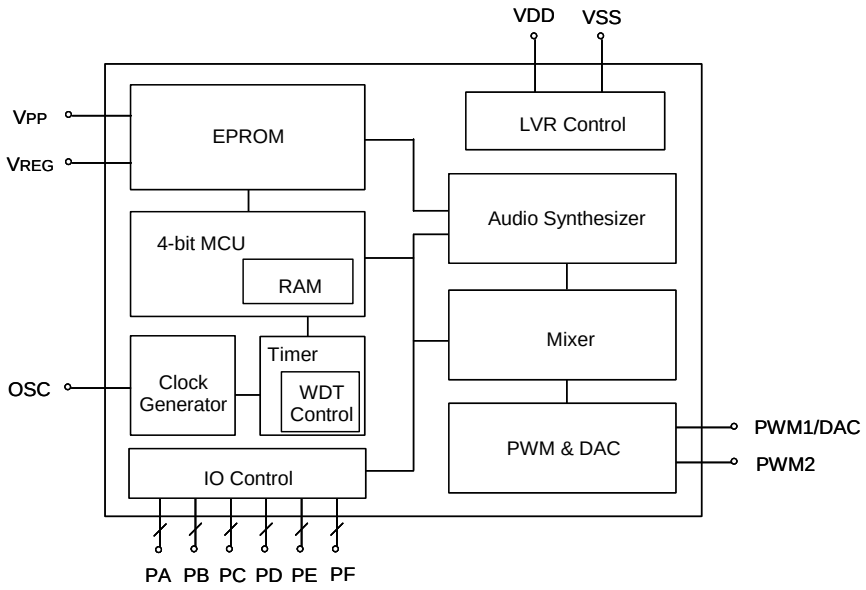
- Wide operating voltage range: 2.0V to 5.5V. *(Same as MaskROM products)*
- 4-bit RISC type micro-controller with 48 instructions.
- 1248Kx10-bit ROM maximum, program and voice data share the same ROM space. The voice duration, ROM size and I/O counts are shown below.

Product (OTP)	Voice Duration (sec) @6kHz	ROM Size (10-bit)	I/O
VLN025-5P	25.0	64k x 10	15 (PA, PB, PC, PD0~2)
VLN055-5P	55.0	136k x 10	15 (PA, PB, PC, PD0~2)
VLN085-5P	85.0	208k x 10	15 (PA, PB, PC, PD0~2)
VLN185-5P	185.0	448k x 10	20 (PA, PB, PC, PD, PE)
VLN345-5P	345.0	832k x 10	20 (PA, PB, PC, PD, PE)
VLN520-5P	518.3	1248k x 10	24 (PA, PB, PC, PD, PE, PF)

- 224x4-bit RAM maximum, divided into 4 pages.
- 1MHz instruction frequency.
- SLOW mode to operate at low power consumption. *(Not suggest using in Timer/Clock application.)*
- HALT mode to save power, less than 1uA@3V standby current.
- Precisely embedded oscillator with build-in resistor (+/- 1%). External resistor to adjust system frequency is optional.
- Low voltage reset (LVR=1.8V), watch-dog reset and I/O port reset are all supported to protect the system.
- One interrupt entrance with an independent stack, multiple interrupt sources.

- Maximum 24 flexible I/Os maximum with optional function: input, output, large current output, IO, floating-type reset, pull-high reset, IR carrier output and large current IR carrier output. For the output port, users can select the normal Drive current output or large Sink current output to directly drive high brightness LED.
- Support Open-Drain (OD) bi-direction IO.
- Infrared output: optional IR carrier frequency and optional data high/low IR output supported.
- Maximum of 4 channels can play simultaneously; each channel can be arbitrarily assigned as speech, tone or midi channel based on the product spec.
- New high fidelity ADPCM speech synthesis algorithm.
- 3 kinds of 256 points, ADSR and Full-Wave instrument waveform provide outstanding midi quality for MIDI.
- 256 steps envelope control for tone and MIDI.
- High quality 9-bit PWM to directly drive speaker, or 10-bit D/A converter audio output to amplify the volume by external audio amplifier for multi-channel MIDI especially.
- Support large PWM current output.
- 16 steps volume control for audio output.
- Quick-IO control supported.
- A unique fast writing mode is provided to speed up OTP writing time.
- A special ICP *(In Circuit Programming)* writing function is supported for user to fabricate PCBA in advance.
- Programmable code protection is provided. *(When the Security-Bit is burnt down, data can't be read.)*
- Various shipping type for different application requirement.

3. BLOCK DIAGRAM



4. PAD DESCRIPTION

Pad Name	ATTR.	Description
V_{REG}	Power	Regulator input. Connect a 0.1uF cap to GND or keep floating.
VDD#	Power	Positive power.
GND#	Power	Negative power.
PA0	I/O	Bit 0 for Port A.
PA1	I/O	Bit 1 for Port A,
PA2~3	I/O	Bit 2~3 for Port A.
PB0~3	I/O	Bit 0~3 for Port B.
PC0~3	I/O	Bit 0~3 for Port C.
PD0~1	I/O	Bit 0~1 for Port D.
PD2/OSC	I/O	Bit 2 for Port D, or External resistor for oscillator input.
PD3	I/O	Bit 3 for Port D. *(PD3 for VLN185-5P, VLN345-5P & VLN520-5P.)*
PE0~2	I/O	Bit 0~2 for Port E. *(PE0~3 for VLN185-5P, VLN345-5P & VLN520-5P.)*
PE3/OSC	I/O	Bit 3 for Port E, or External resistor for oscillator input.
PF0~2	I/O	Bit 0~2 for Port F. *(PF0~3 for VLN520-5P only.)*
PF3/OSC	I/O	Bit 3 for Port F, or External resistor for oscillator input.
PWM1/DAC	O	PWM1 output or DAC output.
PWM2	O	PWM2 output,

* VLN025-5P, VLN055-5P, VLN085-5P: OSC pad is shared with PD2.

* VLN185-5P, VLN345-5P: OSC pad is shared with PE3.

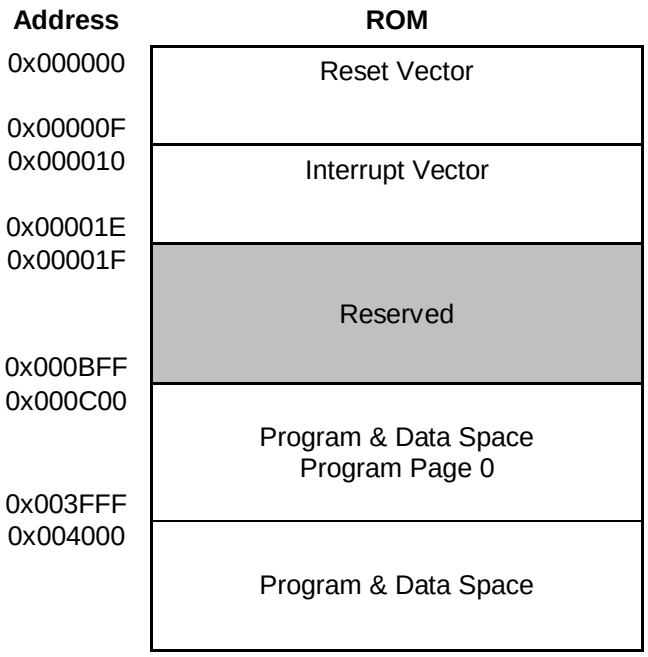
* VLN520-5P : OSC pad is shared with PF3.

5. MEMORY ORGANIZATION

There are maximum 1248K words EPROM, 224 nibbles of RAM and 19 nibbles of dedicated system control register. The registers are divided into 11 nibbles of system registers and 8 nibbles of memory registers. Besides, there are several registers without address allocation, and they can only be accessed by the special instructions. One of the registers is RAM page register (PG), and the others are audio control registers.

5.1 ROM

A large program/data/voice single ROM is provided, and its structure is shown below. The reserved region contains system information and can't be utilized by users. The program page is limited by the unconditional branch instruction: JMP and CALL. Because it can only handle 14-bit length address of ROM, the program page size is 16K words.



5.2 RAM

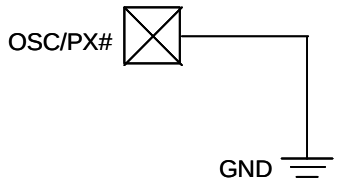
Each page of RAM contains 56 nibbles, and VLN5P serial provides 224 nibbles of 4 pages. The page number (PG) register of RAM defined by the MPG instruction, and its initial value is 0. Because the memory space is shared with the memory registers (address=0x00~0x07), the address for RAM is 0x08~0x3F.

In addition to the immediate addressing mode, the indexed addressing mode is also supported. The page and address of the indexed RAM should be stored into RPT1 and RPT0 first, and users can read from or write in the XMD memory register to realize the indexed ROM access.

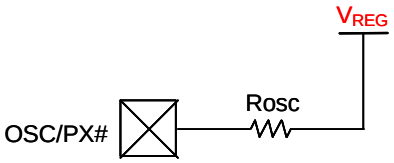
6. Clock Generator

The clock generator is a Ring oscillator, and users can select the internal resistor (INT-R) or the external resistor (EXT-R). A precise INT-R oscillator is provided, and its accuracy is up to ±1%.

For VLN025-5P ~ 5P085A bodies if OSC/PD2 pad is optioned as PD2 I/O function, or for VLN185-5P ~ 345-5P bodies if OSC/PE3 pad is optioned as PE3 I/O function or for VLN520-5P body if OSC/PF3 is optioned as PF3 I/O function, there is only INT-R, and EXT-R is disabled. When this pad is optioned as OSC function oppositely, INT-R or EXT-R can be determined by the configurations below. And the OSC pad must be connected to V_{REG} rather than V_{DD} when using EXT-R.



INT-R Oscillator Connection



EXT-R Oscillator Connection

7. IO PORTS

There are most 24 I/O ports, designated as PAx through PFx, and x=0~3. All the I/O ports can be configured as input, output, or IO port (bi-direction). For the input port, we provide an internal pull-high register option for convenience. For the output port, users can also option its initial value as low or high according to your application circuit. Besides, users can also enable the large current option for each output port to get a larger sink current. The bi-direction IO port can be an input or output by its register value, and users can option the bi-direction IO with a pull-high resister or without a pull-high resister (Open-Drain). When the register equals 0, it is an output and can only output zero. When the register equals 1, it is a weak pull-high or floating (Open-Drain) so that it also can be considered as an input port with/without a pull-high resistor. Users also can enable the large sink current option of an IO port.

The PX0 port means the PA0, PB0, PC0, PD0, PE0 or PF0 port can also be optioned as an external reset pin or an infrared (IR) output pin. A reset port can possess a pull-high resister or not, and an IR port can be initial low or high and also large sink current or not.

The pull-high resister of all the I/O ports has two kinds of option: weak and strong. The weak one is about 850KΩ @3V for normal application and the strong one is about 480KΩ @3V usually for key matrix function. When users configure the weak or strong pull-high resister, the pull-high resisters of all I/O ports are set as the option value.

For VLN025-5P ~ VLN085-5P bodies, PD2 pad is shared with external OSC pad. When users enable external OSC function, PD2 function will be disabled. For VLN185-5P ~ VLN345-5P bodies, PE3 pad is shared with external OSC pad. When users enable external OSC function, PE3 function will be disabled. For VLN520-5P body, PF3 pad is shared with external OSC pad. When users enable external OSC function, PF3 function will be disabled.

8. AUDIO SYNTHESIZER

There are 1-ch voice and 2-ch tone or 4-ch speech/Midi, and all modes are auto-played back by hardware. Different channel mode possesses different hardware structure. It provides a hardware mixer to mix the channel data. The mixer contains a mixer control register MIX. 1-ch ~ 4-ch voice and/or Midi are all configurable by programming the MIX Two audio output stages: DAC and PWM are supported.

8.1 Voice

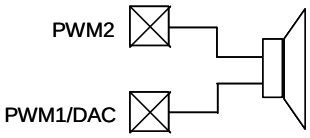
A voice channel includes a PFLG, a VPR, a voice decoder, a QIO control code generator and an 8-bit sample rate timer (TM) whose timer clock source (TCS) is fixed to 1MHz. It supports PCM and encoded ADPCM speech data.

8.2 Tone or Midi

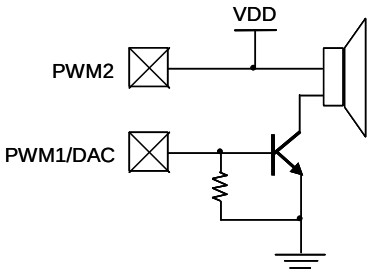
A tone channel includes a TM and an 8-bit envelope (ENV). A Midi channel includes a PFLG, a VPR, a TM, an ENV, a timbre skipper and a multiplier, which multiplies the Midi data and the envelope value held by the ENV. The timbre skipper is used to fulfill the higher octave pitch playing. The hardware multiplier is dedicated to the Midi channel, and users can't operate it by any instruction.

8.3 Audio Output

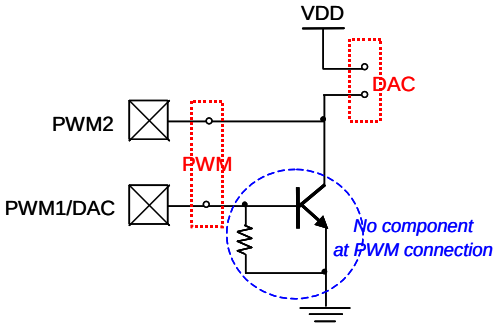
By setting the AUD register, PWM or DAC can be easily chosen as the audio output stage. Besides, it provides a pad detecting mechanism. The pad detecting mechanism detects the PWM2 pad during the reset initialization period, and sets the initial value of the audio output register as PWM if the PWM2 connection is floating, or sets the initial value of the audio output register as DAC if the PWM2 connection is high. In conclusion, connect the speaker to PWM1 and PWM2 only if using PWM, otherwise connect PWM2 to VDD if using DAC. Since the mechanism sets only the initial value of AUD, don't change the value of the AUD register if the pad detecting mechanism is adopted.



PWM Output Connection



DAC Output Connection



PWM/DAC Connection Together

When using the PWM output, we provide an option of normal PWM current or large PWM current for different customer demand. The large PWM consumes more current and makes sound louder.

8.4 Volume Control

Both PWM and DAC support 16 steps hardware volume control by the VOL register. It also provides a DAC current control (CC) option to adjust the DAC current for different BJT properties.

9. ELECTRICAL CHARACTERISTICS

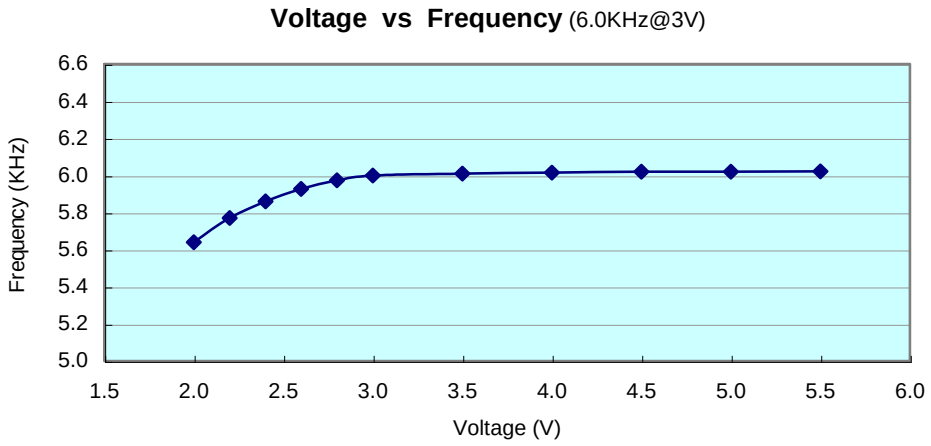
9.1 Absolute Maximum Rating

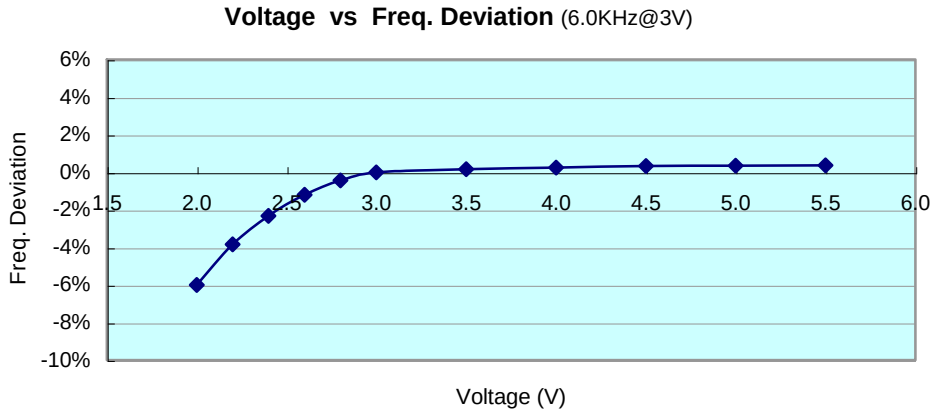
Symbol	Parameter	Rated Value	Unit
Vdd - Vss	Supply voltage	-0.5 ~ +6.0	V
Vin	Input voltage	Vss–0.3V ~ Vdd+0.3	V
Top	Operating Temperature	0 ~ +70 (can use -20~+70)	°C
Tst	Storage Temperature	-25 ~ +85	°C

9.2 DC Characteristics

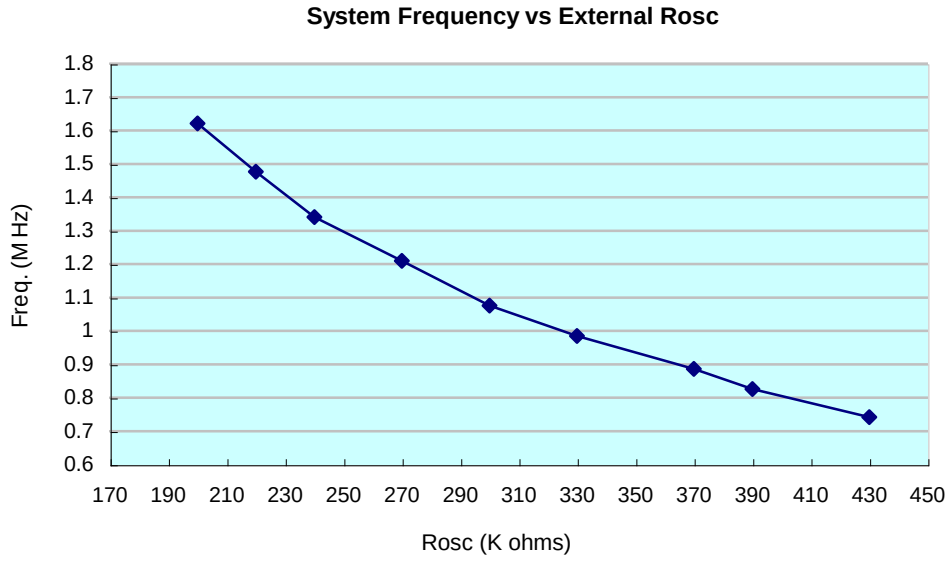
Symbol	Parameter		VDD	Min.	Typ.	Max.	Unit	Condition
VDD	Operating voltage			2.0	3	5.5	V	1 MHz
Isb	Supply current	Halt mode	3			1	uA	Sleep, no loading
			4.5			1		
Isl		Slow mode	3		150		uA	1ms interrupt, no load
			4.5		350			
Iop		Operating mode	3		2		mA	1MHz, no loading
			4.5		2.4			
Iil	Input current (Internal pull-high)	Weak (850k ohms)	3		-3.5		uA	Vil=0v
			4.5		-10			
		Strong (480k ohms)	3		-7			
			4.5		-20			
Ioh	Output high current		3		-10		mA	Voh=1.0V
			4.5		-22			Voh=2.2V
Iol	Output low current (Normal current)		3		10		mA	Vol=2.0V
			4.5		20			Vol=2.5V
Iol	Output low current (Large current)		3		20		mA	Vol=2.0V
			4.5		40			Vol=2.5V
I_{PWM}	PWM output current (Normal)		3		60		mA	Load=8 ohms
			4.5		100			
I_{PWM}	PWM output current (Large)		3		70		mA	Load=8 ohms
			4.5		117			
△F/F	Frequency deviation by voltage drop (1MHz)		3		2		%	Fosc(3.0v)-Fosc(2.4v) / Fosc(3v)
			4.5		0.5			Fosc(4.5v)-Fosc(3.0v) / Fosc(4.5v)
△F/F	Frequency lot deviation (1MHz)		3	-1		1	%	Fmax(3.0v)-Fmin(3.0v) / Fmax(3.0v)
Fosc	Oscillation Frequency		-	0.90	1	1.05	MHz	VDD=2.0~5.5V

9.3 Voltage vs. Frequency





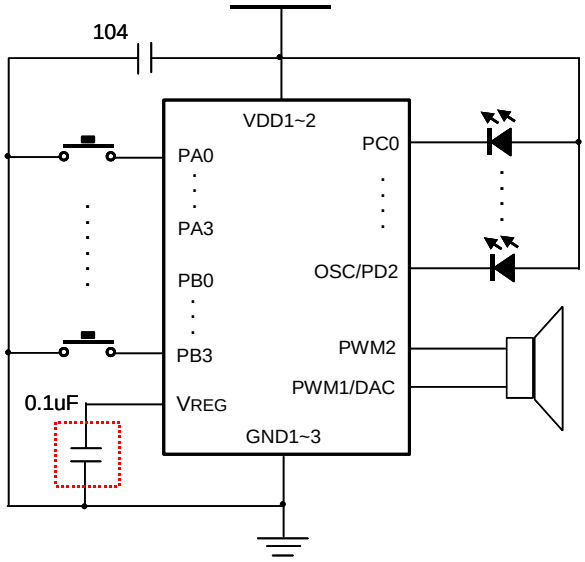
9.4 System Frequency v.s. External Rosc



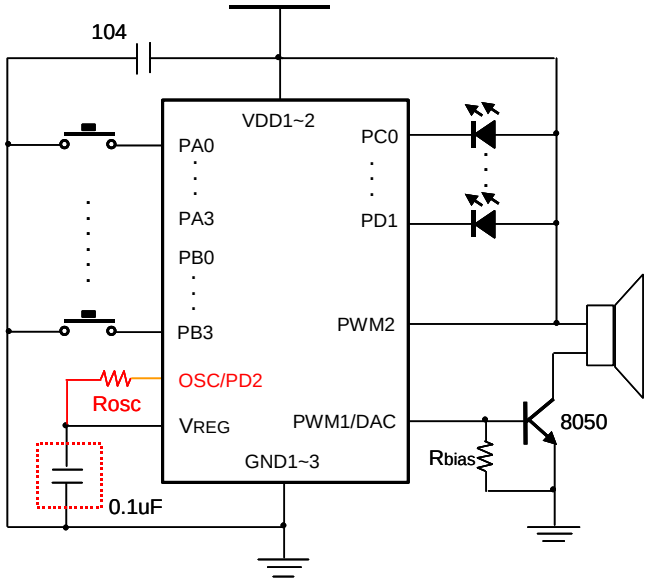
10. APPLICATION

10.1 VLN025-5P, VLN055-5P, VLN085-5P

(1) INT-R, PWM ***(OSC/PD2 is optioned as PD2 pad)***

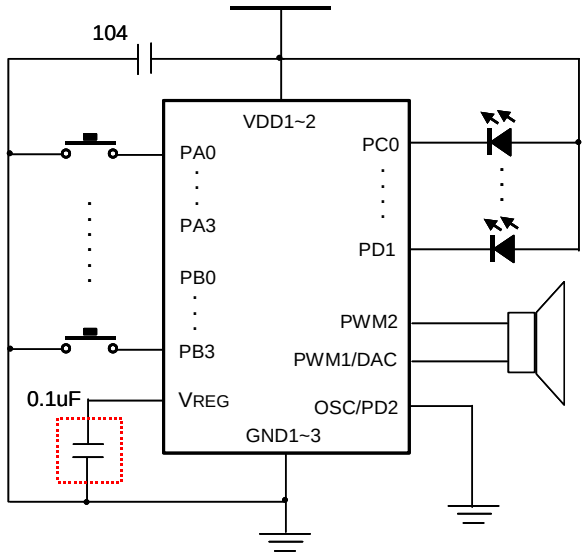


(2) EXT-R, DAC ***(OSC/PD2 is optioned as OSC pad)***



Note: While using external OSC, the OSC pad must be connected to V_{REG} rather than VDD.

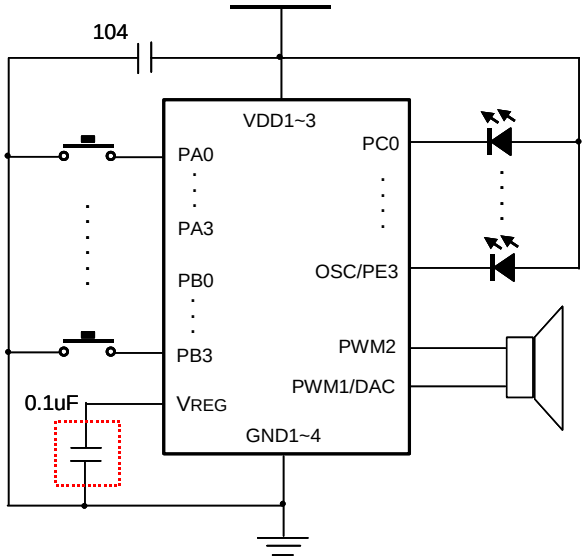
(3) INT-R, PWM ***(OSC/PD2 is optioned as OSC pad)***



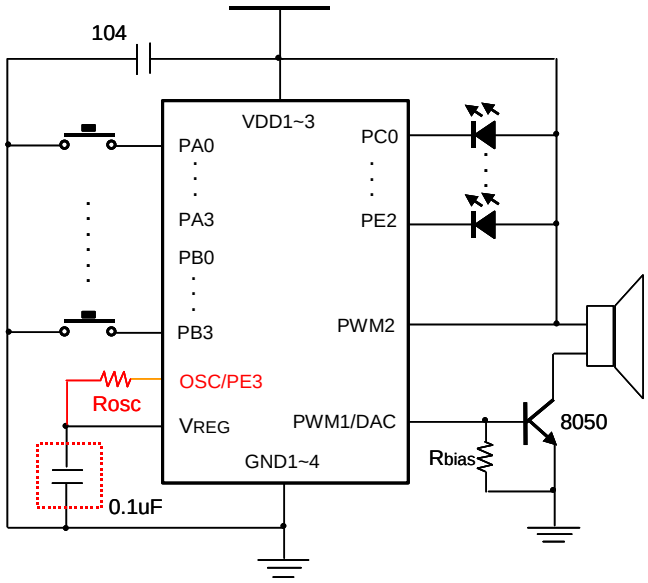
Note: At high voltage of 4.5V or higher voltage, V_{REG} maybe need to connect to GND with a 0.1uF cap for less power noise. At 3V, V_{REG} don't need to connect any capacitor and can be kept this pad floating to save a capacitor.

10.2 VLN185-5P, VLN345-5P

(1) INT-R, PWM ***(OSC/PE3 is optioned as PE3 pad)***

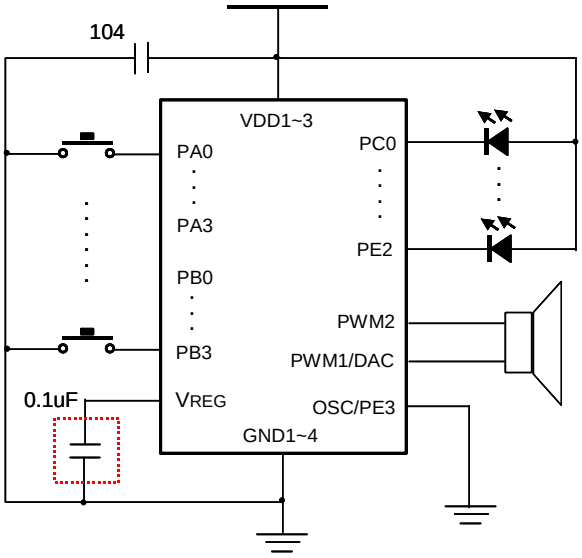


(2) EXT-R, DAC ***(OSC/PE3 is optioned as OSC pad)***



Note: While using external OSC, the OSC pad must be connected to V_{REG} rather than VDD.

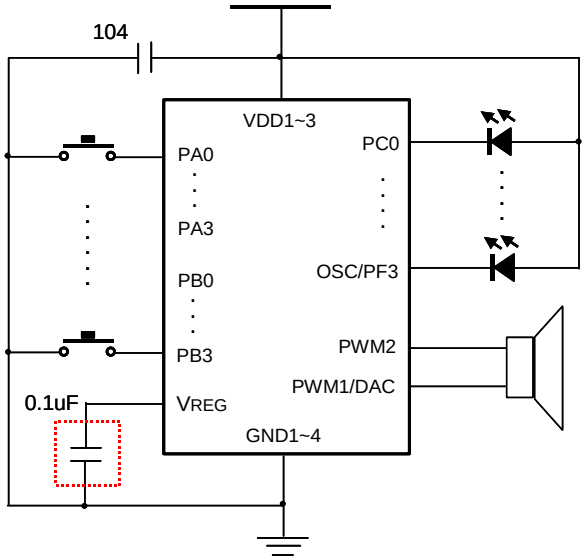
(3) INT-R, PWM ***(OSC/PE3 is optioned as OSC pad)***



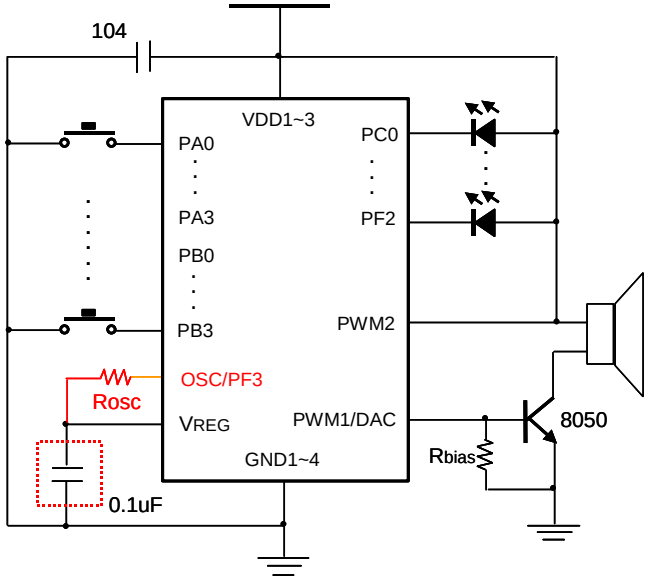
Note: At high voltage of 4.5V or higher voltage, V_{REG} maybe need to connect to GND with a 0.1uF cap for less power noise. At 3V, V_{REG} don't need to connect any capacitor and can be kept this pad floating to save a capacitor.

10.3 VLN520-5P

(1) INT-R, PWM ***(OSC/PE3 is optioned as PE3 pad)***

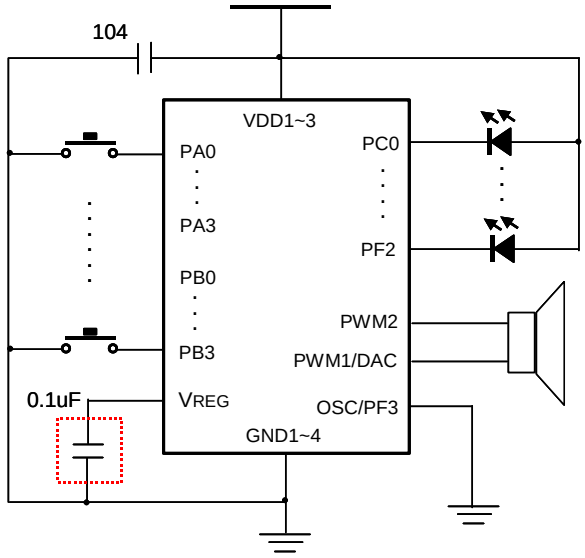


(2) EXT-R, DAC ***(OSC/PE3 is optioned as OSC pad)***



Note: While using external OSC, the OSC pad must be connected to V_{REG} rather than VDD.

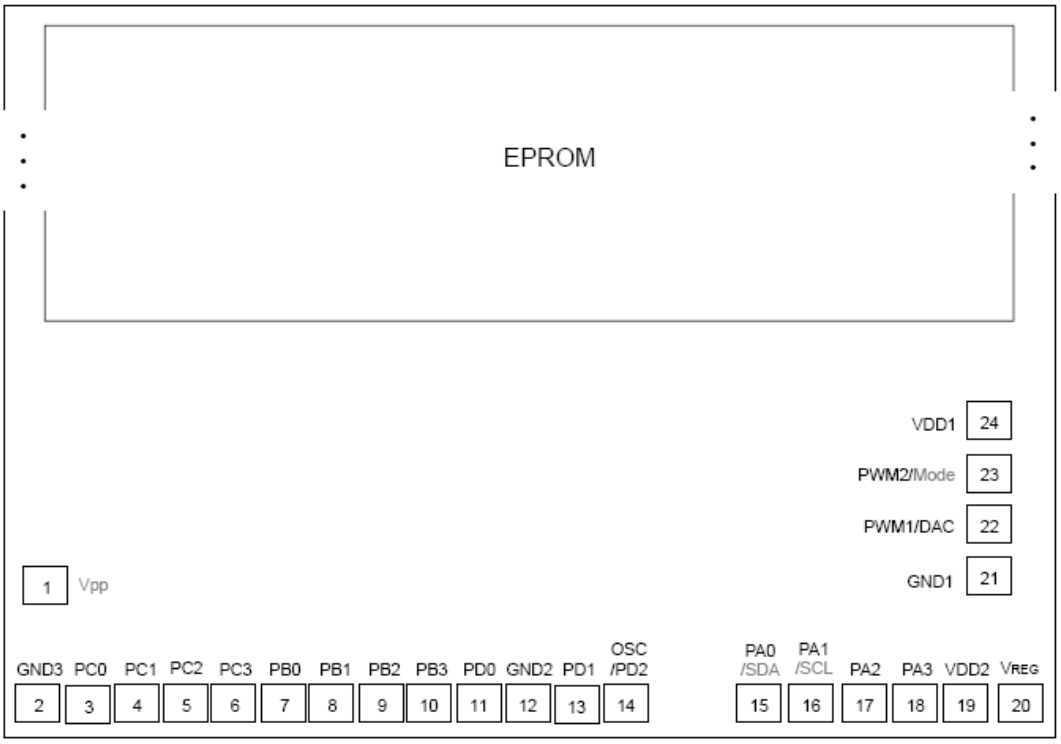
(3) INT-R, PWM ***(OSC/PE3 is optioned as OSC pad)***



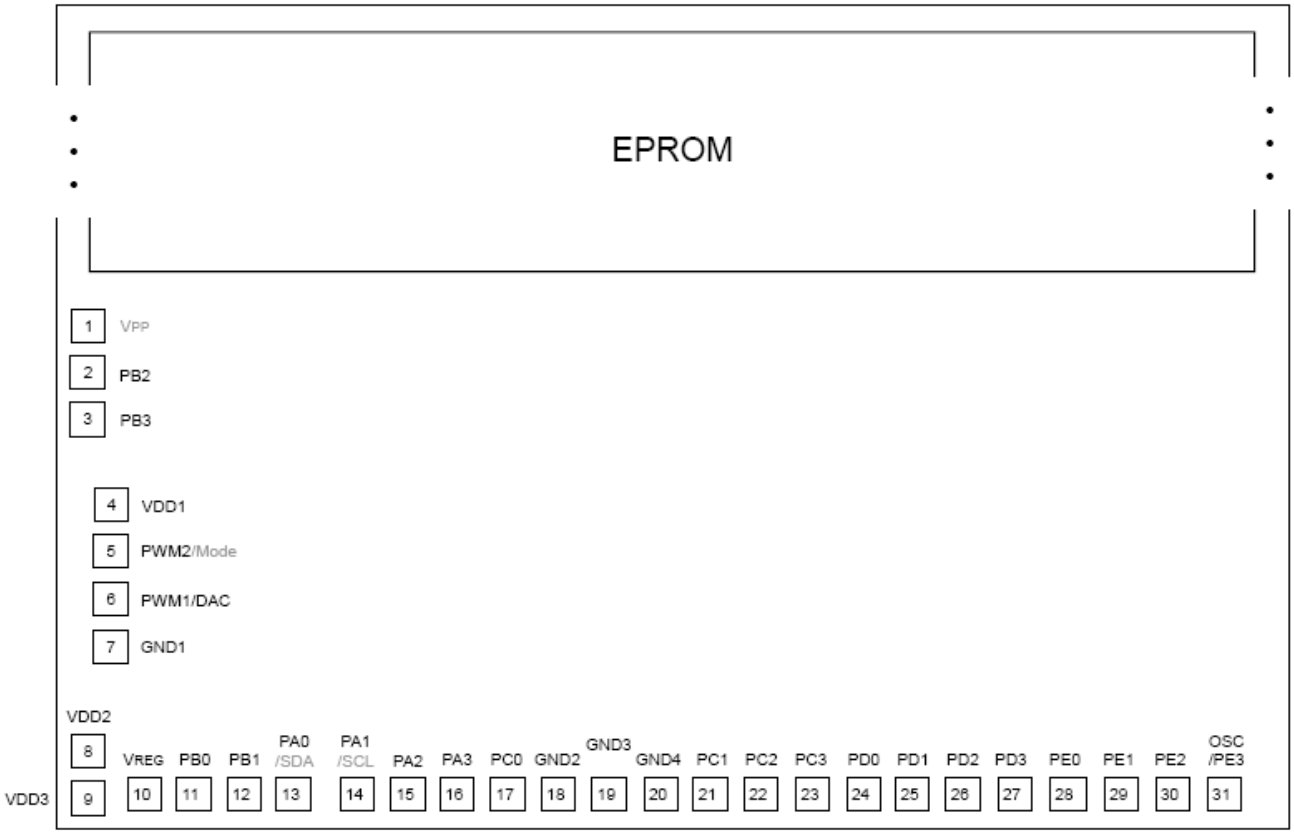
Note: At high voltage of 4.5V or higher voltage, V_{REG} maybe need to connect to GND with a 0.1uF cap for less power noise. At 3V, V_{REG} don't need to connect any capacitor and can be kept this pad floating to save a capacitor.

11. DIE PAD DIAGRAM

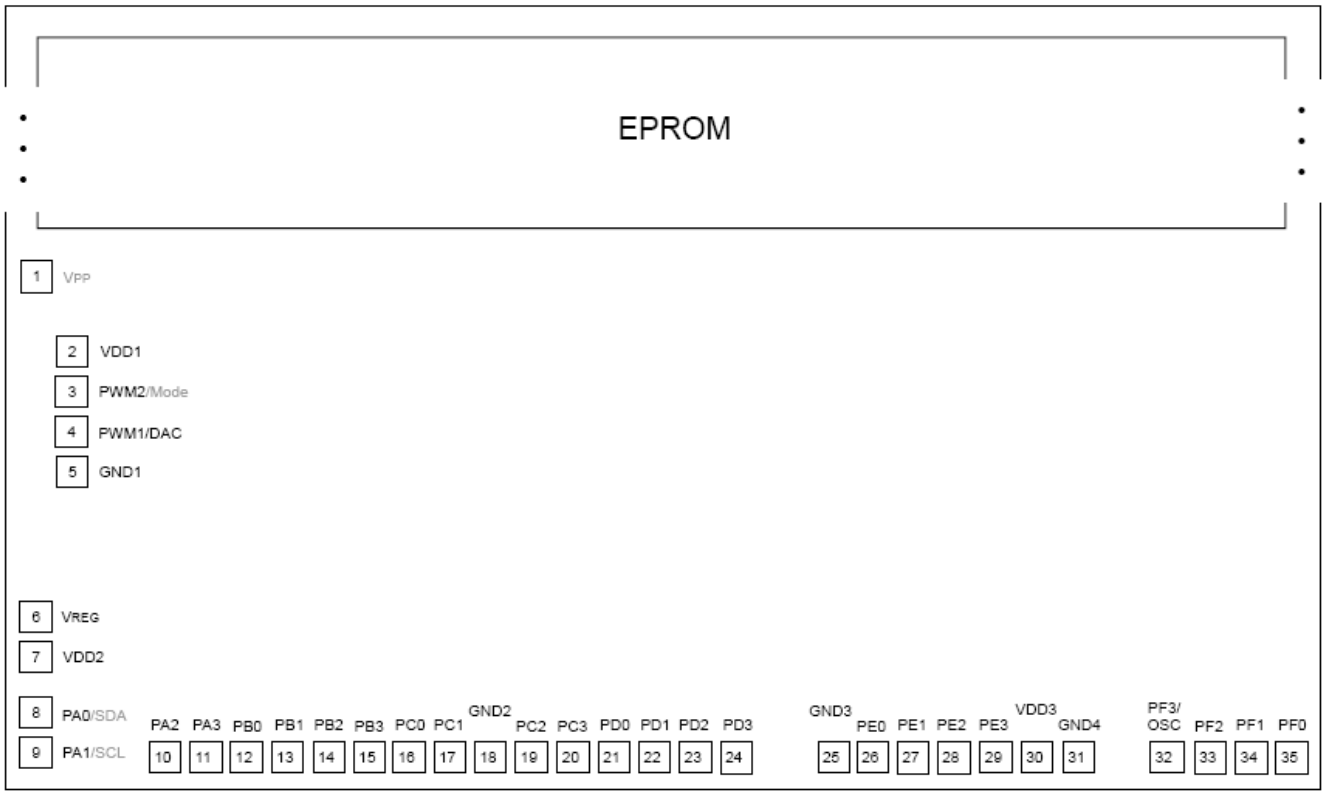
11.1 VLN025-5P, VLN055-5P, VLN085-5P



11.2 VLN185-5P, VLN345-5P



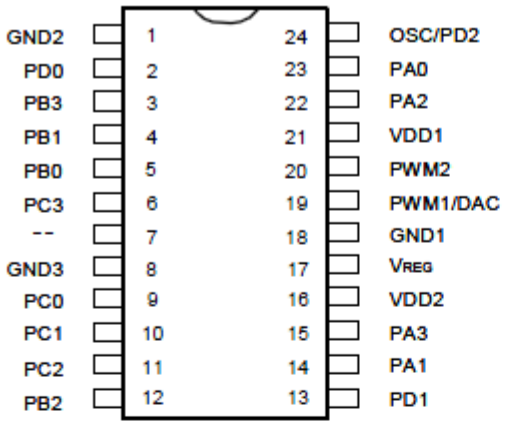
11.3 VLN520-5P



12. COB

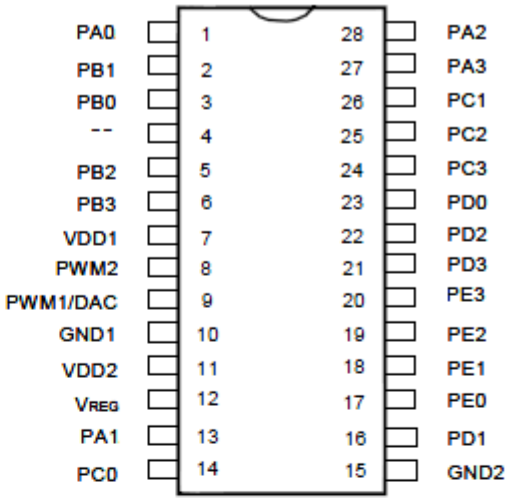
13. PACKAGE PIN ASSIGNMENT

24-pin SOP (300mil)



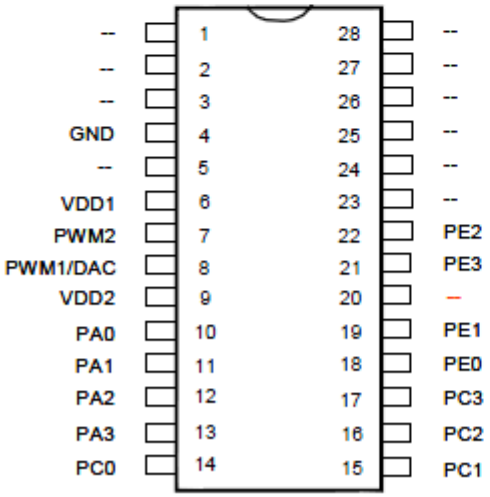
VLN025-5S24
VLN055-5S24
VLN085-5S24

28-pin SOP (300mil)



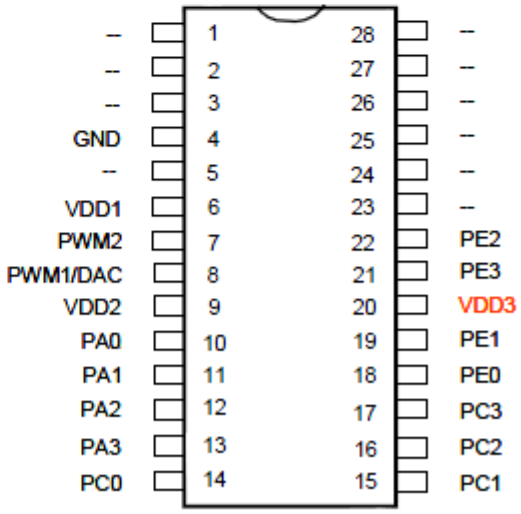
VLN185-5S28

28-pin SOP (300mil)

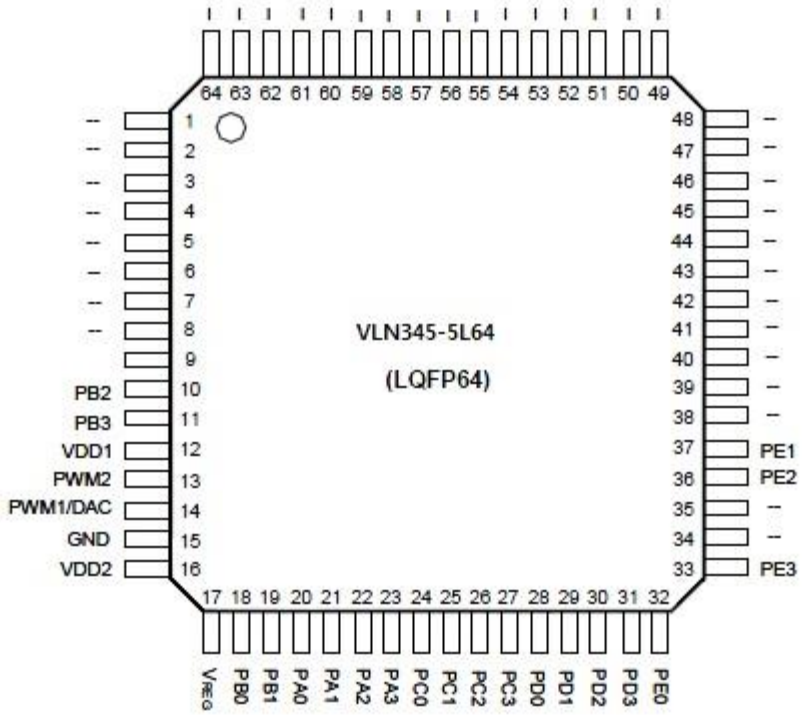


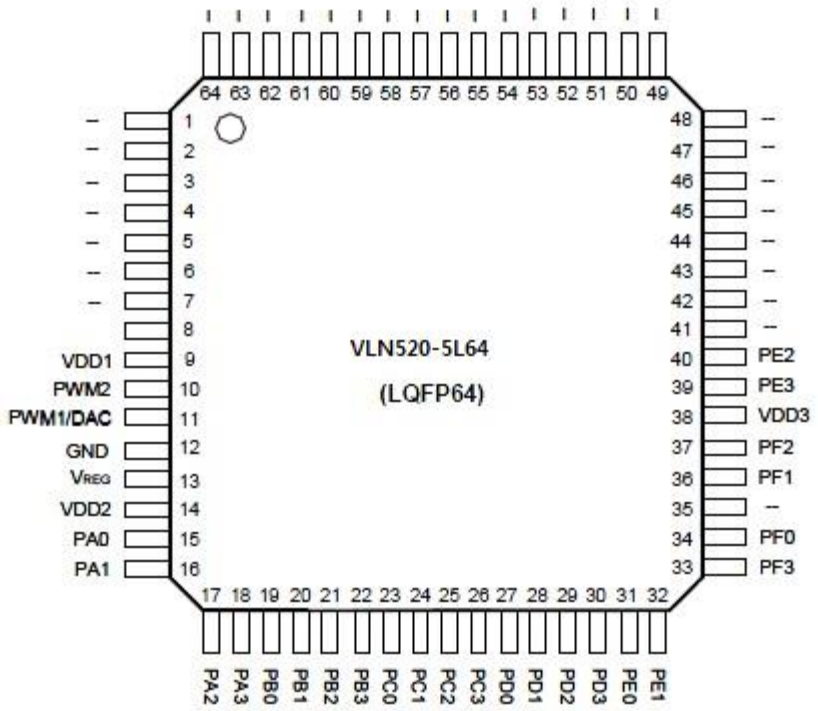
VLN345-5S28

28-pin SOP (300mil)



VLN520-5S28

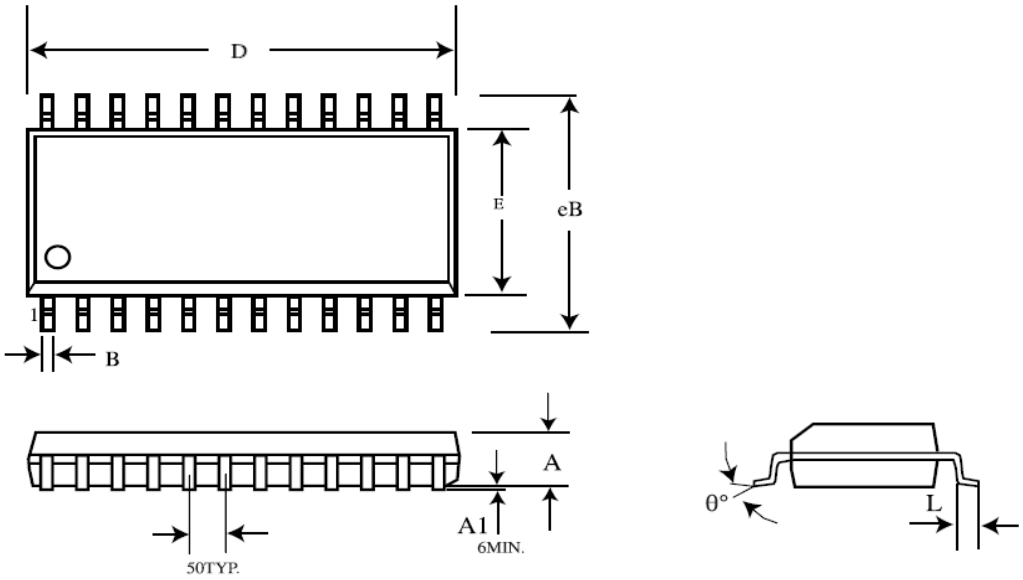




" – " means "Not Connection" (N/C).

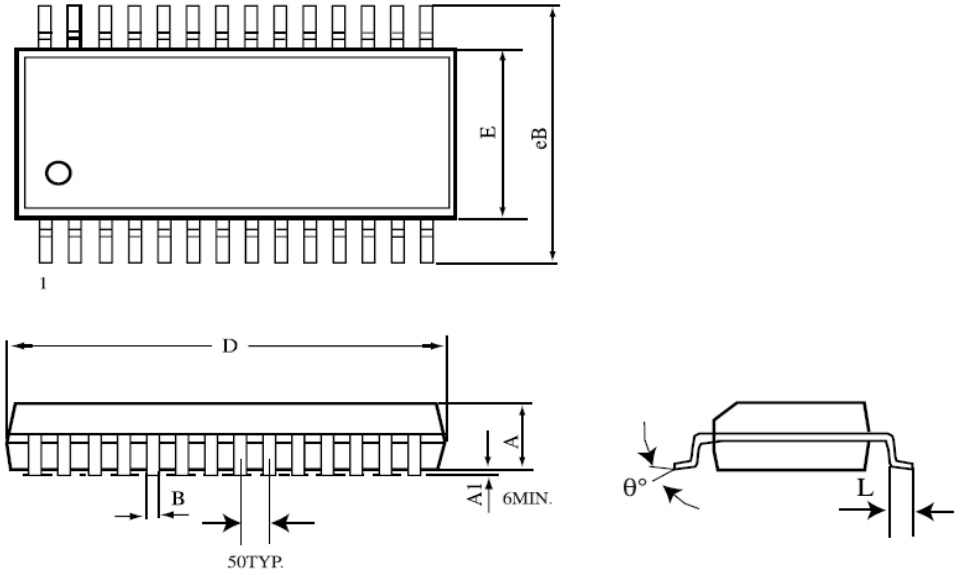
14. PACKAGE DIMENSION

24-Pin Plastic SOP (300 mil)



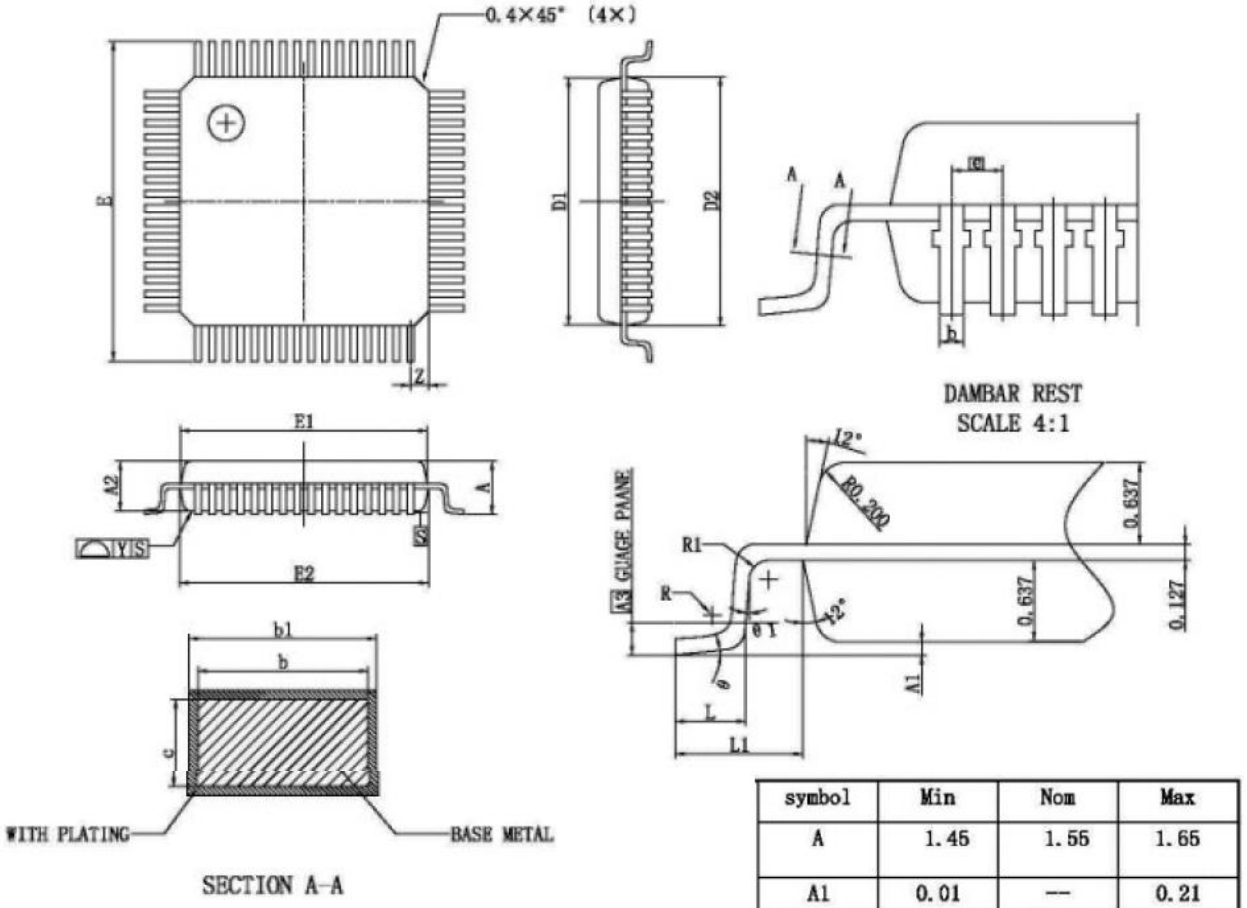
Sym.	Dimension in mils			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	98	100	102	2.489	2.540	2.591
A1	6	- - -	- - -	0.152	- - -	- - -
B	12	16	20	0.305	0.406	0.508
D	606	608	610	15.392	15.443	15.494
E	298	300	302	7.569	7.620	7.671
eB	406	410	414	10.312	10.414	10.516
L	25	- - -	- - -	0.635	- - -	- - -
θ°	0°	4°	8°	0°	4°	8°

28-Pin Plastic SOP (300 mil)



Sym.	Dimension in mils			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	90	92	94	2.286	2.337	2.388
A1	6	- - -	- - -	0.152	- - -	- - -
B	12	16	20	0.305	0.406	0.508
D	703	705	707	17.856	17.907	17.958
E	293	295	297	7.442	7.493	7.544
eB	406	410	414	10.312	10.414	10.516
L	25	- - -	- - -	0.635	- - -	- - -
θ°	0°	4°	8°	0°	4°	8°

64-Pin LQFP (7mm x 7mm)



symbol	Min	Nom	Max
A	1.45	1.55	1.65
A1	0.01	—	0.21
A2	1.3	1.4	1.5
A3	—	0.254	
b	0.13	0.18	0.23
b1	0.14	0.20	0.26
c	—	0.127	—
D1	6.85	6.95	7.05
D2	6.9	7.00	7.10
E	8.8	9.00	9.20
E1	6.85	6.95	7.05
E2	6.9	7.00	7.10
e	—	0.4	—
L	0.43	—	0.71
L1	0.90	1.0	1.10
R	0.1	—	0.25
R1	0.1	—	—
θ	0	—	10°
θ1	0	—	—
y	—	—	0.1
Z	—	0.5	—

NOTE:
1. All dimensions are in mm.
2. Dim D1/D2 & E1/E2 does not include plastic flash. Flash: Plastic residual around body edge after dejunk/singulation.
3. Dim b does not include dambar protrusion/intrusion.
4. Plating thickness 0.005~0.015mm.

15. ORDERING INFORMATION

P/N	Shipping Type	Remarks
VLN025-5S24	SOP-24	Width 300 mil
VLN055-5S24	SOP-24	Width 300 mil
VLN085-5S24	SOP-24	Width 300 mil
VLN185-5S28	SOP-28	Width 300 mil
VLN345-5S28	SOP-28	Width 300 mil
VLN520-5S28	SOP-28	Width 300 mil
VLN345-5L64	LQFP-64	Quad 7 x 7 mm
VLN520-5L64	LQFP-64	Quad 7 x 7 mm