

VLNxxx_3P Series (OTP for VLN3)

5 I/O Single-Chip Speech Synthesizer

Version 1.6

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1. GENERAL DESCRIPTION

The VLN3P series are single-chip voice synthesizing CMOS IC. They are embedded EPROM architecture, and OTP (One Time Programmable) IC that are designed to support MaskROM products. There are 6 bodies: VLN010-3P8, VLN016-3P8, VLN035-3P8, VLN065-3P8, VLN087-3P8 and VLN115-3P8. Each body has one input and four I/O pins except VLN010-3P8 with one input and two I/O pins. Through accurate internal oscillation of +/- 1% tolerance, an external R_{osc} is unnecessary. There is only one PWM output for voice. Thus any external component is not required. Using the same speech algorithm of VLN3P, customer's speech data can be written into EPROM by different code data.

2. FEATURES

- (1). Wide operating voltage: 1.6V ~ 6.4V.
- (2). There are 6 bodies. Corresponding to different VLN3 series, the supported ROM size in Hex and speech duration at 6kHz are as following.

	<i>VLN010-3P8</i>	<i>VLN016-3P8</i>	<i>VLN035-3P8</i>	<i>VLN065-3P8</i>	<i>VLN087-3P8</i>	<i>VLN115-3P8</i>
<i>VLN3P</i>	8.60s	15.20s	32.68s	67.63s	87.29s	120.06s

- (3). Five I/O pins: OKY1 can only be input pin. Other OKY2/O4, IO1, IO2 and IO3 can be either input or output pin (Mask option).

※ Note: There are only three I/O pins for VLN010-3P8 (OKY, IO1, IO2).

- (4). The total voice duration can be partitioned up to maximum 1008 *Voice Sections*. Each *Voice Section* length is flexible and each maximum or minimum *Voice Section* length is unlimited.
- (5). Total maximum 1008 *Voice Steps* are available for 64 *Voice Sentences*. OKY1, OKY2/O4, IO1, IO2 and IO3 can be assigned 32, 29, 1, 1 and 1 *Sentences* independently. Each *Step* can be specified one *Voice Section* and enable/disable IO1, IO2, IO3, OKY2/O4 output option if IO_x is set as output.
- (6). Only build in an accurate internal oscillator of +/- 1% tolerance, no external R oscillator. It can support different play speed option of VLN3P individually.

- (7). I/O mapping table.

<i>VLN3P</i>	<i>OKY1</i>	<i>OKY2/O4</i>	<i>IO1</i>	<i>IO2</i>	<i>IO3</i>

- (8). Input option for input pin: (Mask option)

- (a). Each input can select Edge/Level, Hold/Unhold and Retrigger/Irretrigger trigger modes.
- (b). Each input can select CDS+300K, CDS, 300K pull-low resistor or Floating type.

(CDS+300K option: Only 300k pull-low resistance at key-pressed, and 100K+300K in parallel pull-low resistance around 75K at key-released. CDS option: Floating at key-pressed, and 100K pull-low resistance at key-released.)

※ Note: VLN3A input type is CDS+300K, CDS, 300K pull-low resistor or Floating type.

- (c). Each input can select Debounce time: Long debounce for push-button. Short debounce for fast switch.
- (d). OKY1 & OKY2/O4 input can select One-Key Sequential or Random for maximum 32 & 29 *Sentences* independently. At One-Key Sequential, the Reset function of playing *Sentence* sequence can be selected or not when other keys are triggered.
- (e). Only one input pin can select Toggle On/Off function (1st Trigger → play, 2nd trigger → stop,).

※ *Note: Input priority is OKY1 > OKY2/O4 > IO1 > IO2 > IO3.*

- (9). All output pins support large-current output and can directly drive high brightness LED. ($I_{ol}=20\text{mA}$ @ $V_{DD}=3\text{V}$)
- (10). There are 9 kinds of output option for all output pins: (Mask option)
 - (a). Stop_Low pulse: Low active stop-pulse output whenever device stop playing.
 - (b). Stop_High pulse: high active stop-pulse output whenever device stop playing.
 - (c). Busy_High active: high active signal output during playing. (Drive output)
 - (d). Busy_Low active: low active signal output during playing. (Sink output)
 - (e). LED 3Hz flash: 3Hz sink signal output to drive LED during playing.
 - (f). LED 6Hz flash: 6Hz sink signal output to drive LED during playing.
 - (g). LED 12Hz flash: 12Hz sink signal output to drive LED during playing.
 - (h). LED dynamic 1/2: according to 1/2 sound level, dynamic sink signal output to drive LED during playing.
 - (i). QIO signal: arbitrary output with voice. For IO1, IO2 and IO3, there are two sets of QIO signal. Each *Voice Step* can select one set of QIO signal. But for OKY2/O4, there is only one set of QIO signal to select.

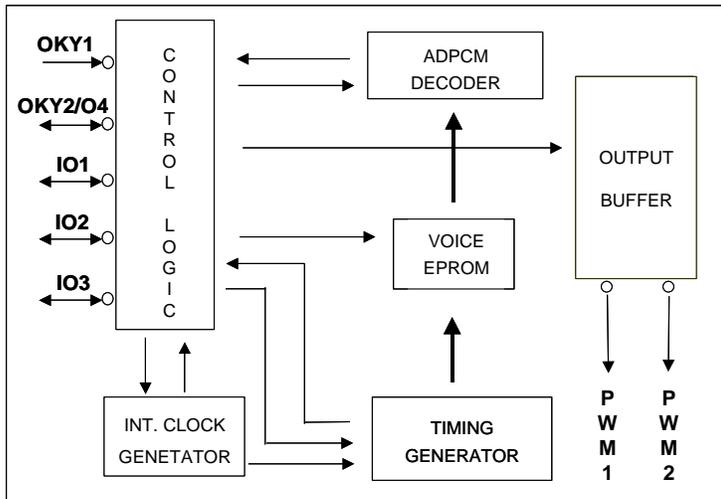
※ *Note: Where (e) ~ (g) is the LED flash rate at 6kHz sample rate. For different play speed, the LED flash rate is different from original 3Hz, 6Hz or 12Hz.*

- (11). Motor-Recover function: User can select this function when using the recovering motor. In this application, IO2 is set as output to control the recovering motor. And the motor recovering sensor must be connected to OKY2/O4 or IO3 to detect the recovering signal. (Mask option)
- (12). STB function: In Edge trigger mode, after any key is continuously pressed for few seconds, IC will enter standby mode automatically to save power. **It's usually used in "Level-Stop" application.** There are 7 kinds of key-pressing time from 1 to 7 seconds. Because play speed will affect the key-pressing time, it causes this key-pressing time inaccurate. **We suggest users MUST confirm this key-pressing time by demo board.** (Mask option)
- (13). **Serial-Trigger function: In Edge/Unhold/Retrigger mode, by using the One-Key Sequential and Reset functions of OKY1 or OKY2 and setting the Debounce time to be short, IC can access external serial clock signal to playback the specific Sentence of OKYx. Usually it cooperates with an external MCU.**
- (14). One PWM output can directly drive speaker or buzzer.
- (15). Low Voltage Reset (LVR) is supported. (**LVR=1.5V**)
- (16). A unique fast writing mode is provided to speed up OTP writing time.

- (17). A special *ICP* (In Circuit Programming) writing function is supported for user to fabricate PCBA in advance.
- (18). Programmable code protection is provided. (*When the Security-Bit is burnt down, data can't be read.*)
- (19). Various shipping type for different application requirement.

(For details of the above functions, please refer to VLN3P datasheet, or contact VOICELAND.)

3. BLOCK DIAGRAM



4. PAD DESCRIPTION

Pad Name	Pad No.	ATTR.	Description
Test	-	I	Test pad. <i>(This pad is only for VLN065-3P8 body.)</i>
OKY1/VPP	1	I	Input pin, active high, or positive high power for programming.
OKY2/O4	2	I/O	Output or input pin. To be input, active high. <i>(N/A for VLN010-3P8)</i>
IO1/SDA	3	I/O	Output or input pin. To be input, active high.
IO2/SCL	4	I/O	Output or input pin. To be input, active high.
IO3	5	I/O	Output or input pin. To be input, active high. <i>(N/A for VLN010-3P8)</i>
V _{REG}	6	Power	Regulator input. Connect a 0.1uF cap to GND or keep floating.
GND	7	Power	Negative power.
VDD	8	Power	Positive power.
PWM1	9	O	PWM output 1.
PWM2/Mode	10	O	PWM output 2, or select programming mode.

5. DEVELOPMENT, DEMONSTRATION & PRODUCTION

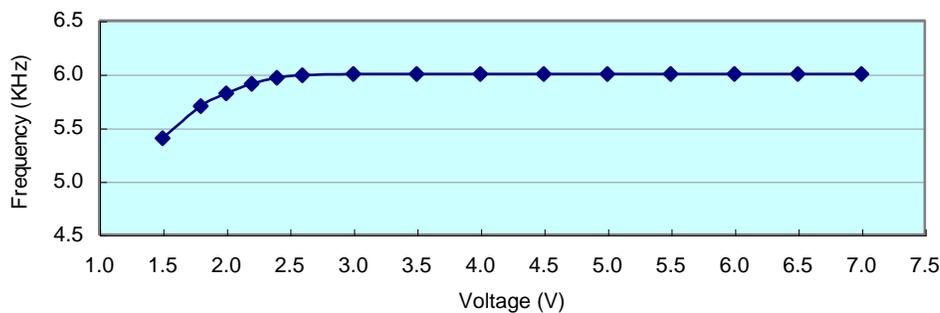
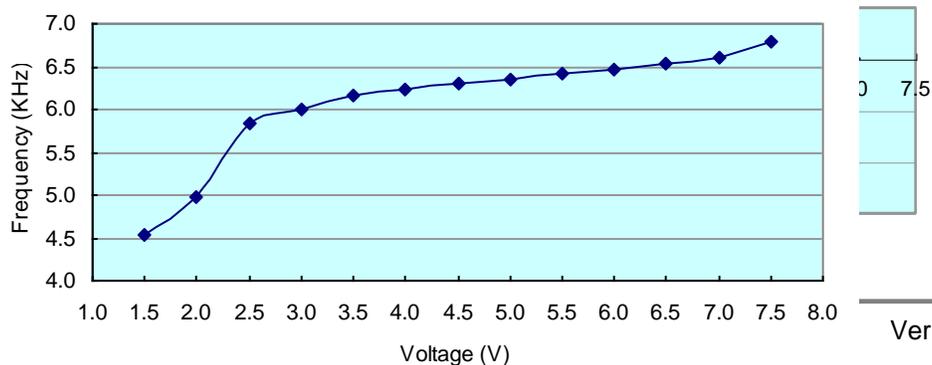
. Customer can request for sample and mass production to VoiceLand.

6. ABSOLUTE MAXIMUM RATING

Symbol	Rating	Unit
VDD~GND	-0.5 ~ +7.0	V
V _{in}	GND-0.3 < V _{in} < VDD+0.3	V
V _{out}	GND < V _{out} < VDD	V
T _{op} (operating)	-0 ~ +70	°C
T _{st} (storage)	-55 ~ +150	°C

7. DC CHARACTERISTICS

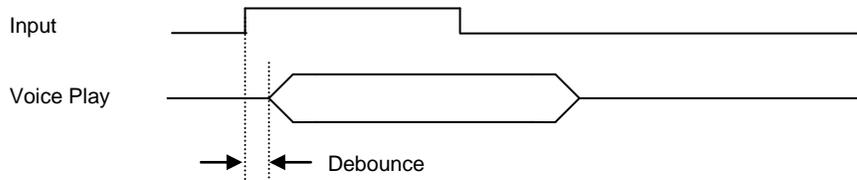
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
VDD	Operating voltage	1.6	3.0	6.4	V	
I _{sb}	Standby current, VDD=3V/4.5V		1		uA	No loading
I _{op}	Operating current	VDD=3V	850			
		VDD=4.5V	1100			
I _{ih}	Input current (1M ohms pull-low, VLN3A only)			3	uA	VDD=3V
				8		VDD=4.5V
I _{ih}	Input current (300k ohms pull-low)			10	uA	VDD=3V
				25		VDD=4.5V
I _{ih}	Input current (100k ohms pull-low)			30	uA	VDD=3V
				80		VDD=4.5V
I _{oh}	Output drive current		-10		mA	VDD=3V, V _{oh} =1.0V
			-20			VDD=4.5V, V _{oh} =2.2V
I _{ol}	Output sink current		20		mA	VDD=3V, V _{ol} =1.0V
			34			VDD=4.5V, V _{ol} =1.0V
I _{oh}	PWM1, PWM2 output current		-65		mA	VDD=3V, V _{oh} =1.5V
I _{ol}			65			VDD=3V, V _{ol} =1.5V
ΔF/F	Frequency deviation by voltage drop	VDD=3V	1		%	$\frac{F_{osc}(3.0v)-F_{osc}(2.4v)}{F_{osc}(3v)}$
		VDD=4.5V	0.1			$\frac{F_{osc}(4.5v)-F_{osc}(3.0v)}{F_{osc}(4.5v)}$
ΔF/F	Frequency lot deviation (VDD=3V)	-1		1	%	$\frac{F_{max}(3.0v)-F_{min}(3.0v)}{F_{max}(3.0v)}$
F _{osc}	Oscillation Frequency	1.31	1.54	1.61	MHz	VDD=1.6~6.4V

Voltage vs Frequency (SR=6.0KHz@3V)

Voltage vs Frequency (6.0KHz@3V)


8. TIMING DIAGRAM

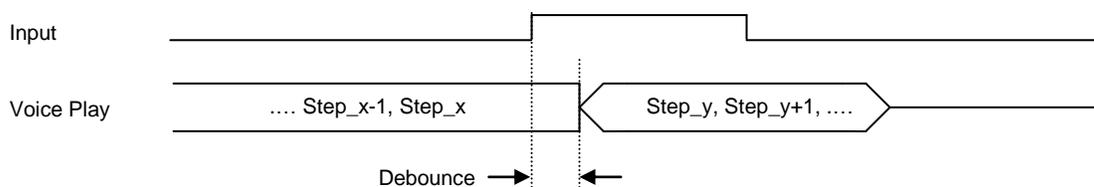
(1) Debounce Time

(a). Trigger while no playing voice



※ Debounce time is configured by 7.2 kHz S.R and the value is fixed. That is, Long debounce=17ms, Short debounce = 42us

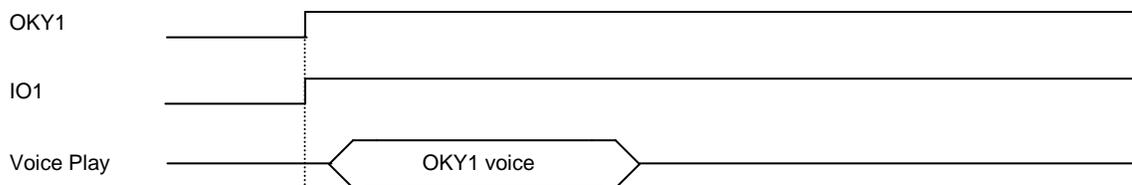
(b). Trigger While playing voice



※ Debounce Time is configured by the S.R. of Step_x. At S.R. = 6kHz, Long debounce = 20ms, Short debounce = 50us

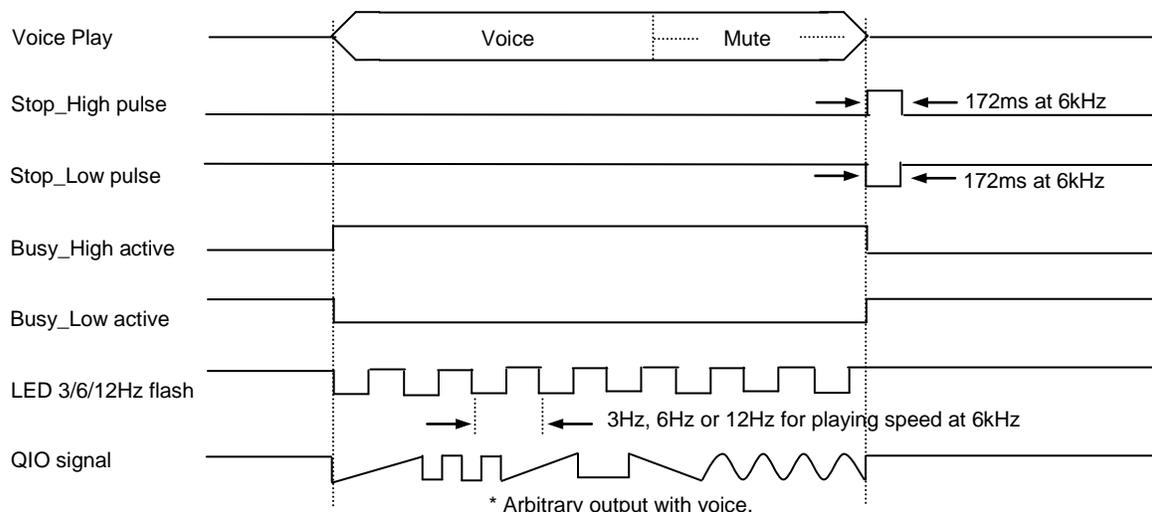
For example, if Step_x S.R. = 8kHz, Long debounce = 20ms*(6k/8k) = 15ms, Short debounce = 50us*(6k/8k) = 37.5us

(2) Input Priority



※ Priority: OKY1 > OKY2 > IO1 > IO2 > IO3

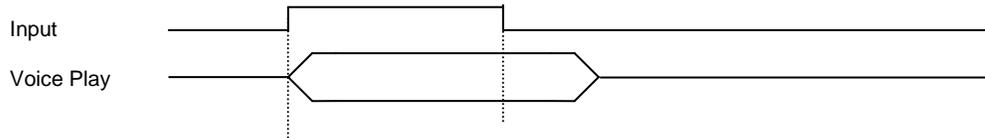
(3) Output Signal (IO1, IO2, IO3, O4)



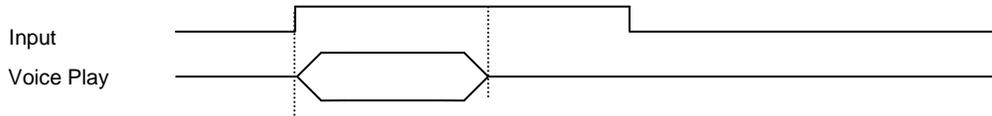
LED dynamic 1/2: When the voice amplitude is higher than 1/2 level, LED will be ON, i.e. output signal is low.

(4) Basic Operation

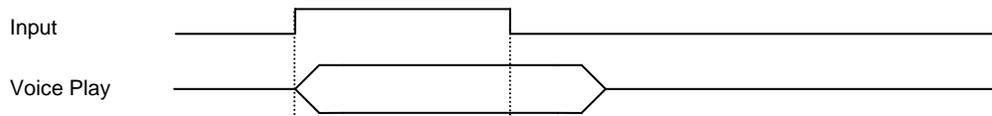
(a). Edge mode, Edge trigger



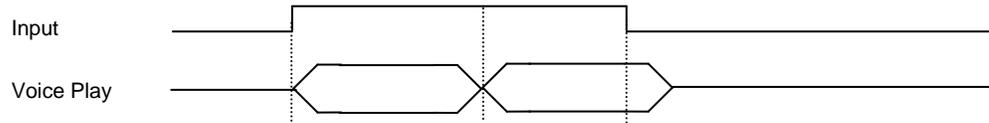
(b). Edge mode, Level trigger



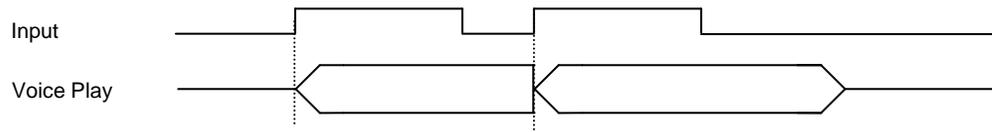
(c). Level mode, Edge trigger



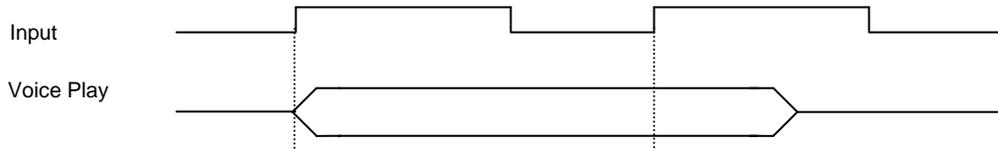
(d). Level mode, Level trigger



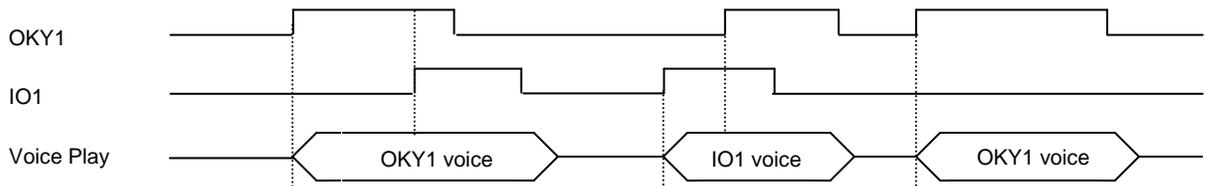
(e). Retrigger mode



(f). Irretrigger mode



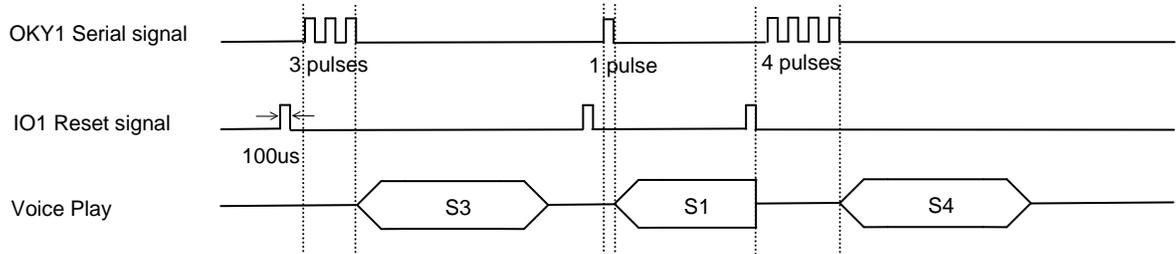
(g). Retrigger mode, first key priority



(5) Advanced Operation

(a). Serial-Trigger Function (All inputs must be set as short debounce)

OKY1 (E/U/R) =S1 S2 S3 S4, IO1 (E/U/R) =S5 (OKY1 Reset is enabled, and S5 is a short mute Sentence)

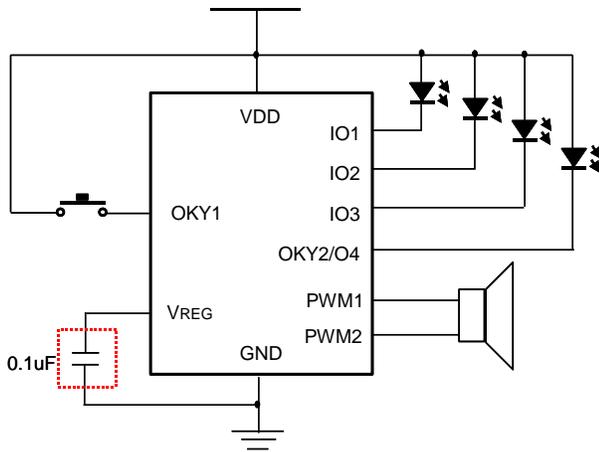


※ The pulse width must be longer than 50us (i.e. short debounce time), and users can set the typical pulse width as 100us.

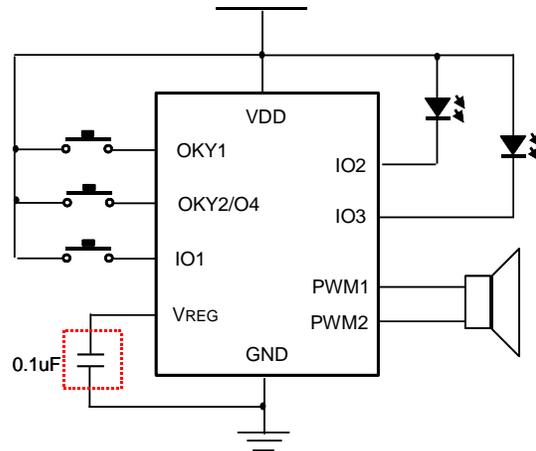
※ The above is the simplest 2-wire control by external MCU. If necessary, user can use 3-wire control with Busy_High output signal to do feedback.

9. APPLICATION

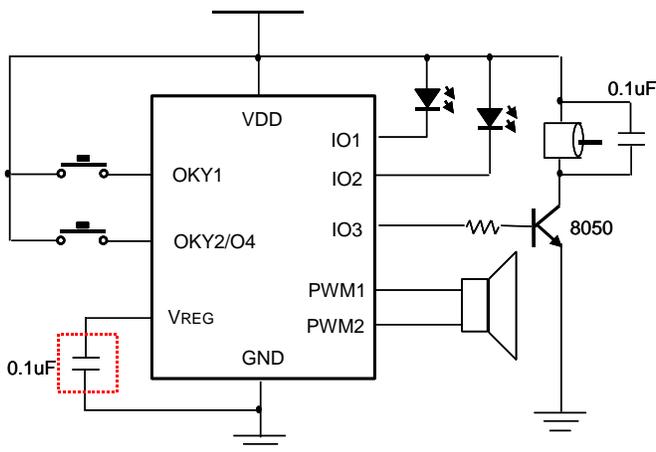
(1) 1 trigger with 4 LEDs (Sink)



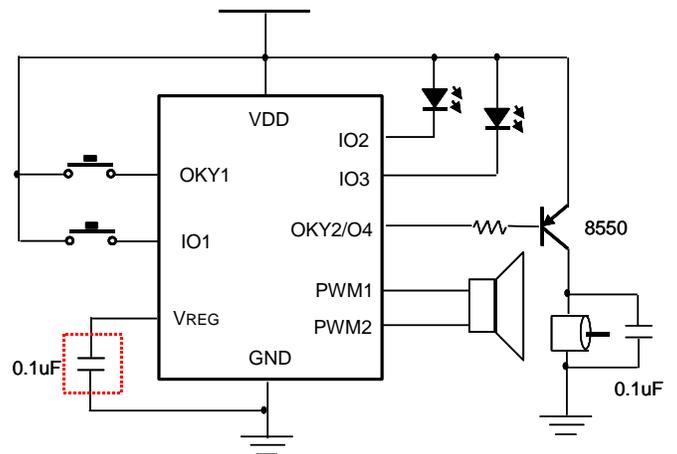
(2) 3 triggers with 2 LEDs (Sink)



(3) 2 triggers with 2 LEDs (Sink) and 1 motor (Drive)



(4) 2 triggers with 2 LEDs (Sink) and 1 motor (Sink)



Note: At high voltage of 4.5V or higher voltage, VREG may be connected to GND with a 0.1uF cap for less power noise. At 3V, VREG doesn't need to connect any capacitor and can be kept this pad floating to save a capacitor.

10. DIE PAD DIAGRAM

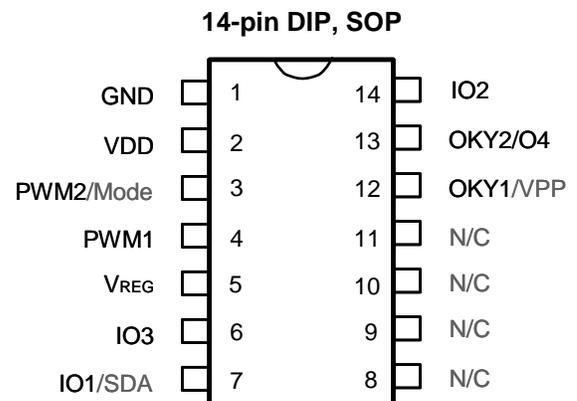
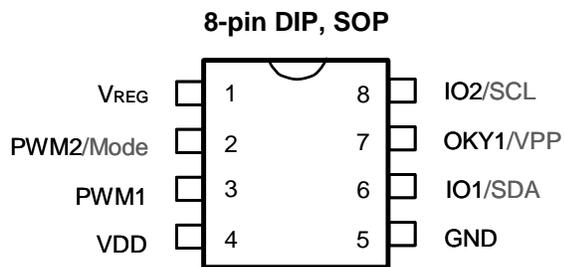


* The IC substrate must be connected to GND or Floating.

**** There is no "Test" pad for OTP bodies.**

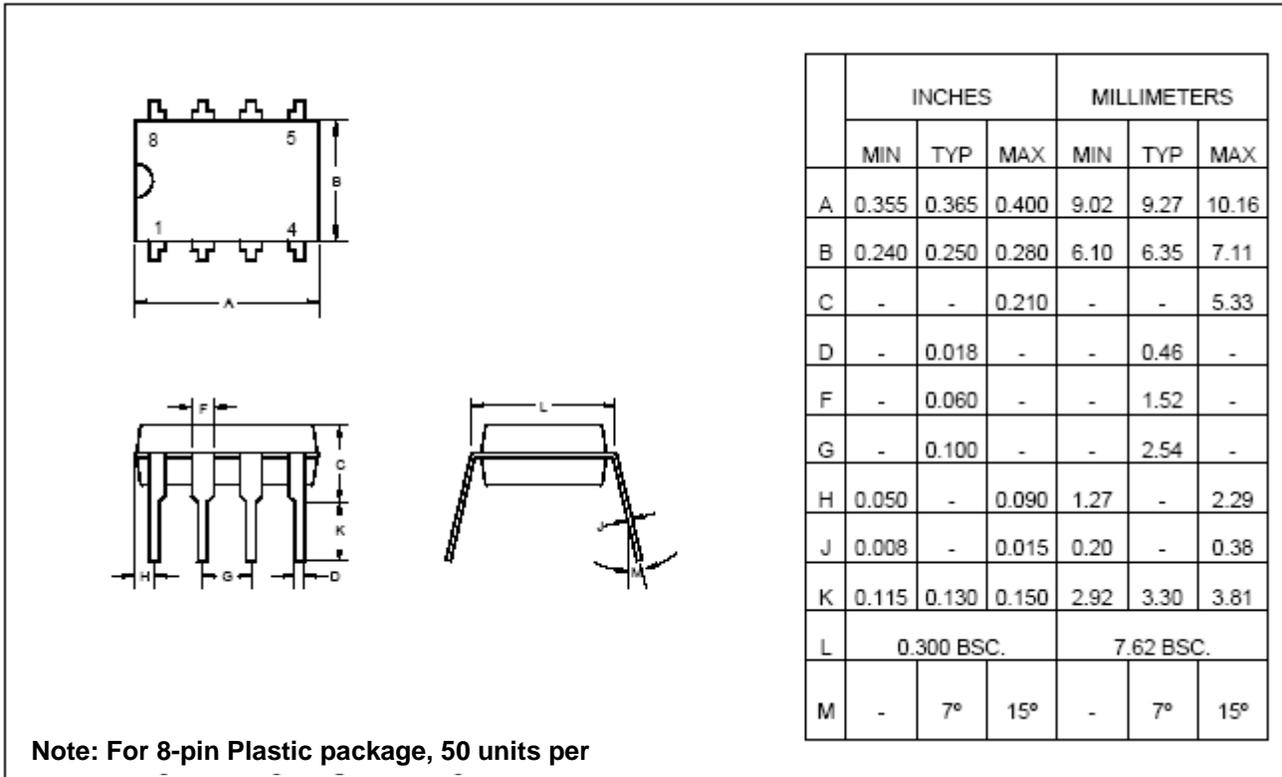
11. COB

12. PACKAGE PIN ASSIGNMENT

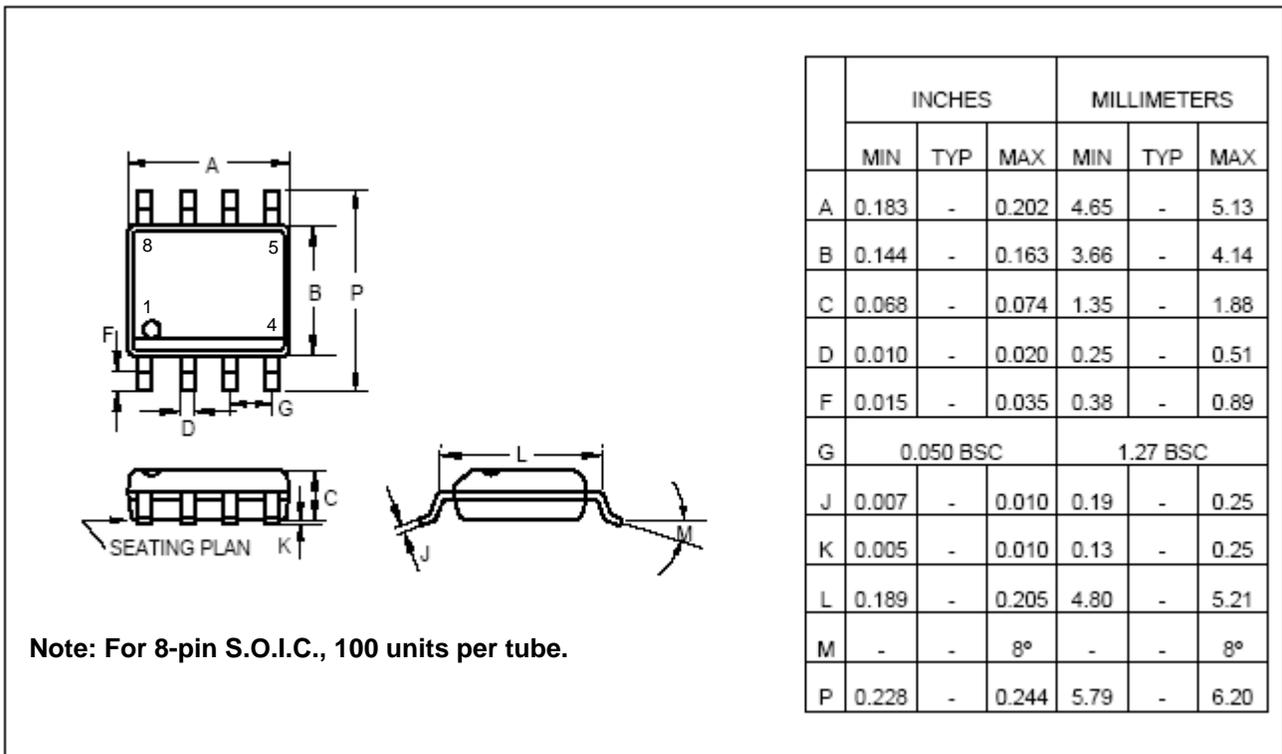


13. PACKAGE DIMENSION

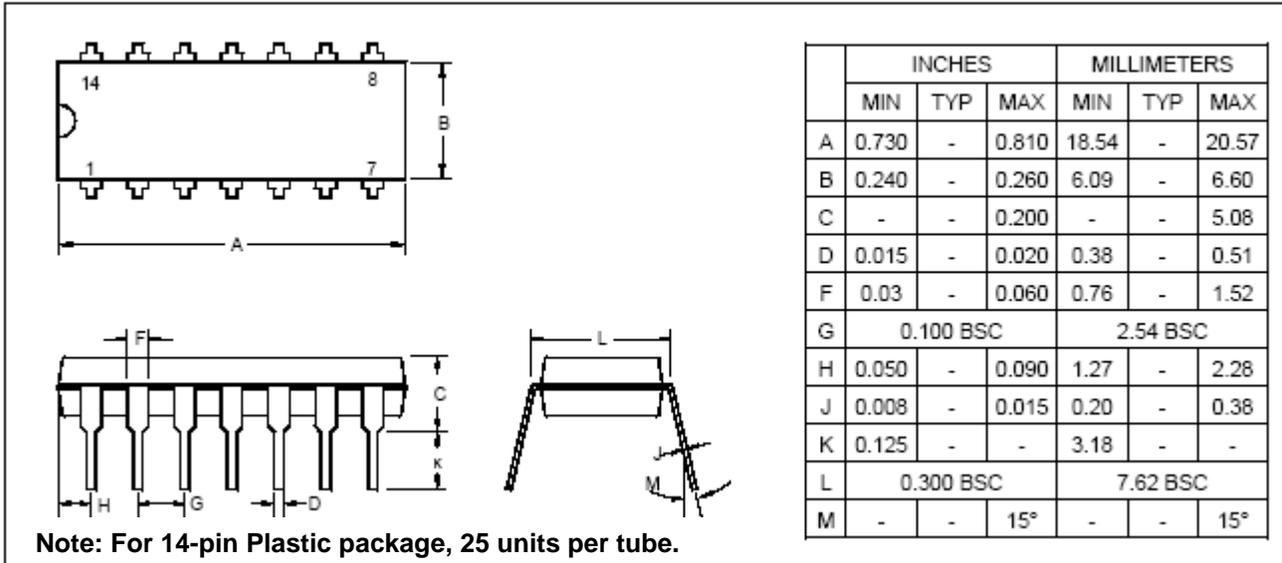
8-Pin Plastic DIP (300 mil)



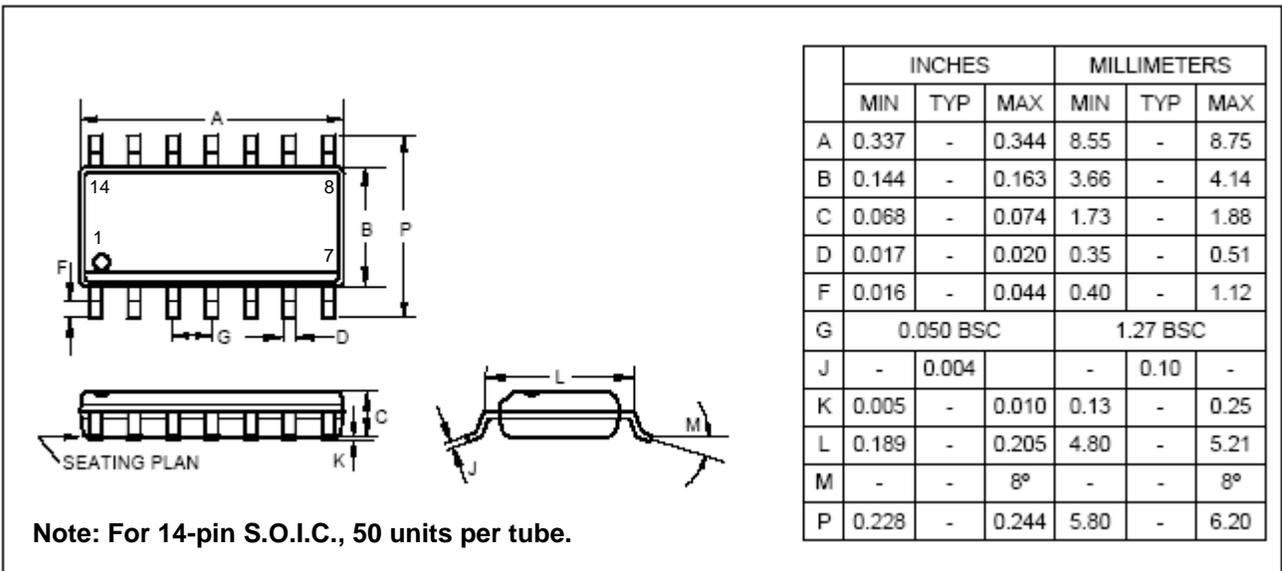
8-Pin Plastic SOP (150 mil)



14-Pin Plastic DIP (300 mil)



14-Pin Plastic SOP (150 mil)



14. ORDERING INFORMATION

<i>P/N</i>	<i>Shipping Type</i>	<i>Remarks</i>
VLN010-3P8	DIP-8	Width 300 mil
VLN010-3S8	SOP-8	Width 150 mil
VLN016-3P8	DIP-8	Width 300 mil
VLN016-3S8	SOP-8	Width 150 mil
VLN016-3P14	DIP-14	Width 300 mil
VLN016-3S14	SOP-14	Width 150 mil
VLN035-3P8	DIP-8	Width 300 mil
VLN035-3S8	SOP-8	Width 150 mil
VLN035-3P14	DIP-14	Width 300 mil
VLN035-3S14	SOP-14	Width 150 mil
VLN065-3P8	DIP-8	Width 300 mil
VLN065-3S8	SOP-8	Width 150 mil
VLN065-3P14	DIP-14	Width 300 mil
VLN065-3S14	SOP-14	Width 150 mil
VLN087-3P8	DIP-8	Width 300 mil
VLN087-3S8	SOP-8	Width 150 mil
VLN087-3P14	DIP-14	Width 300 mil
VLN087-3S14	SOP-14	Width 150 mil
VLN115-3P8	DIP-8	Width 300 mil
VLN115-3P14	DIP-14	Width 300 mil

*1 *VLN115-3P8 doesn't support SOP-8 & SOP-14 package.*