

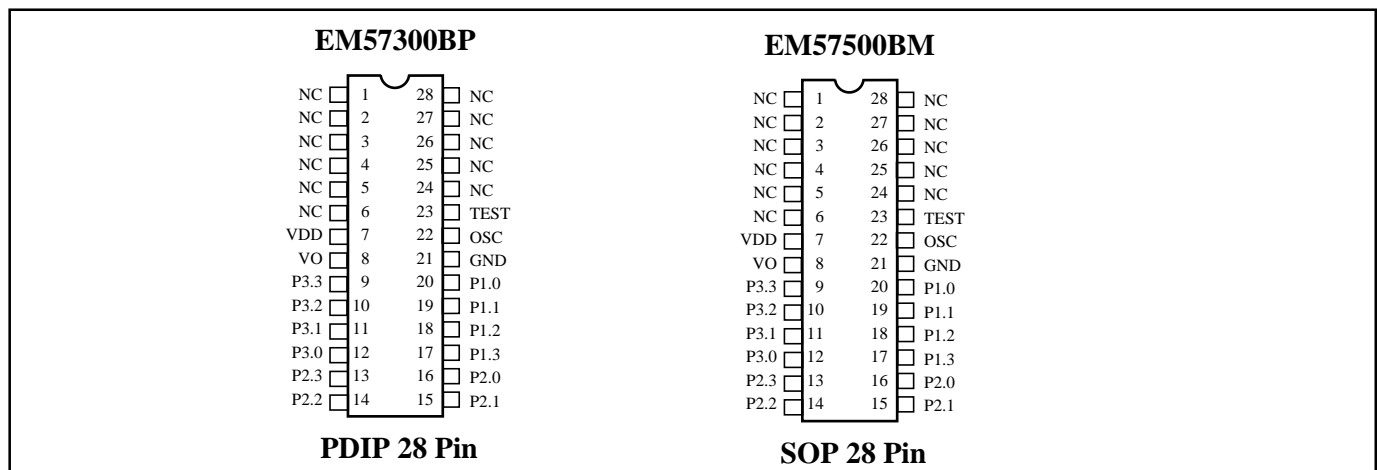
## GENERAL DESCRIPTION

EM57000 is a series of single chip Voice/Dual tone Melody/Dual tone Sound Effect synthesizer ICs. It contains one 4-bit input port (provided for EM57100 and above), two 4-bit I/O ports and a tiny controller. User's applications, such as section combination, trigger modes, control outputs, keyboard matrix, and other logic functions, are easily implemented by programming through its tiny controller.

## FEATURES

- Single power supply 2.4 V ~ 5 V.
- Wide range of ROMs :  
EM57001 - 10Kx10 bits,  
EM57100 - 16Kx10 bits,  
EM57200 - 32Kx10 bits,  
EM57300 - 64Kx10 bits,  
EM57400 - 128Kx10 bits,  
EM57500 - 256Kx10 bits,  
EM57600 - 512Kx10 bits,  
EM57700 - 1024Kx10 bits.
- One 4-bit input port (provided for EM57100 and above), two 4-bit I/O ports.
- 16x4 bits RAM for EM57001,  
32x4 bits RAM for EM57100~EM57500,  
128x4 bits RAM for EM57600 and above.
- 8K (maximum) program ROM for EM57001~EM57500.  
32K (maximum) program ROM for EM57600 and above.
- One 6-bit timer overflow control.
- PCM, ASPCM synthesizer and dual tone melody/sound effect generator.
- 4K~32K Hz playing speed for voice play-back.
- Multiple tempos for dual tone melody/sound effect play-back.
- Variable beats for dual tone melody/sound effect play-back.
- Multiple levels of volume control.
- Fixed current D/A output to drive external connected transistor for voice output.
- A pin ( except EM57001, EM57400 ) can be programmed as an IR communication pin which generate 38KHZ carrier.

## PIN ASSIGNMENTS



## PIN DESCRIPTIONS

Symbol	I/O	Function
P1.0*	I	Bit 0 of Port 1.
P1.1*	I	Bit 1 of Port 1.
P1.2*	I	Bit 2 of Port 1.
P1.3*	I	Bit 3 of Port 1.
P2.0	I/O	Bit 0 of Port 2.
P2.1	I/O	Bit 1 of Port 2.
P2.2	I/O	Bit 2 of Port 2.
P2.3	I/O	Bit 3 of Port 2.
P3.0	I/O	Bit 0 of Port 3.
P3.1	I/O	Bit 1 of Port 3.
P3.2	I/O	Bit 2 of Port 3. IR Tx.
P3.3	I/O	Bit 3 of Port 3. Flash with volume output.
V <sub>DD</sub>	I	Positive power supply.
OSC	I	Oscillation component connection pin.
TEST	I	For testing only.
V <sub>SS</sub>	I	Negative power supply.
VO	O	Voice output.

\* : provided for EM57100 and above

## ABSOLUTE MAXIMUM RATINGS

Items	Sym.	Min.	Max.	Unit
Supply Voltage	V <sub>DD</sub> -V <sub>SS</sub>	-0.3	6.0	V
Input Voltage	V <sub>IN</sub>	V <sub>SS</sub> -0.3	V <sub>DD</sub> +0.3	V
Operating Temperature	T <sub>OP</sub>	-20	70	°C
Storage Temperature	T <sub>STG</sub>	-55	+125	°C

## ELECTRICAL CHARACTERISTICS (V<sub>DD</sub> = 3V, 25°C unless otherwise specified)

Parameter	Sym.	Min.	Typ.	Max.	Unit	Condition
Operating voltage	V <sub>DD</sub>	2.4	3.0	5.1	V	
Standby current	I <sub>DDs</sub>	-	-	1.0	μA	V <sub>DD</sub> =3V
Operating current	I <sub>DDO</sub>	-	-	280	μA	V <sub>DD</sub> =3V, No load
Drive current of P2,P3	I <sub>OD</sub>	1.0	-	-	mA	V <sub>DD</sub> =3V, V <sub>O</sub> =2.4V
Sink current of P2, P3	I <sub>OS</sub>	1.6	-	-	mA	V <sub>DD</sub> =3V, V <sub>O</sub> =0.4V
Input current of P1*	I <sub>IH</sub>	-	3.0	10.0	μA	V <sub>DD</sub> =3V
Output current of VO	I <sub>VO</sub>	2.0	3.0	4.0	mA	V <sub>DD</sub> =3V, V <sub>O</sub> =0.7V (Step 7)
Oscillation resistor	R	-	1.0	-	MΩ	V <sub>DD</sub> =3V
		-	100	-	KΩ	For EM57600HXR
Oscillator frequency	F <sub>osc</sub>	-	1.0	-	MHz	V <sub>DD</sub> =3V

\* : provided for EM57100 and above

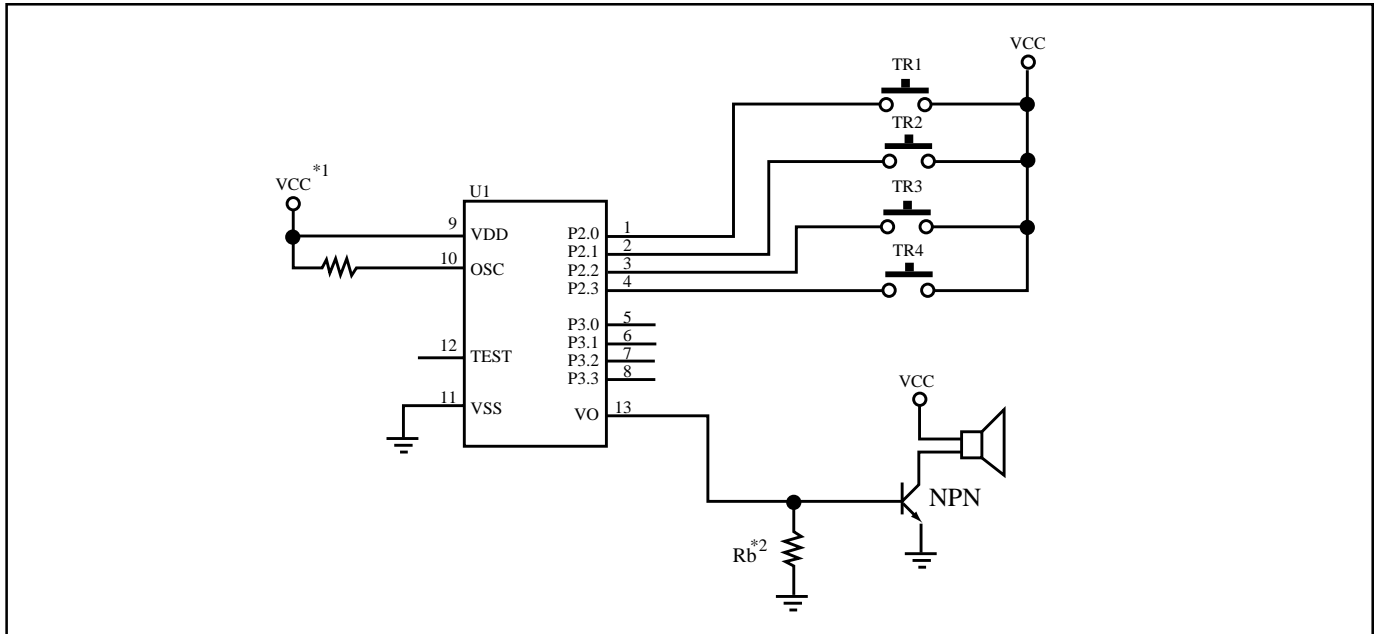
\* This specification are subject to be changed without notice.

## APPLICATION CIRCUIT FOR EM57001

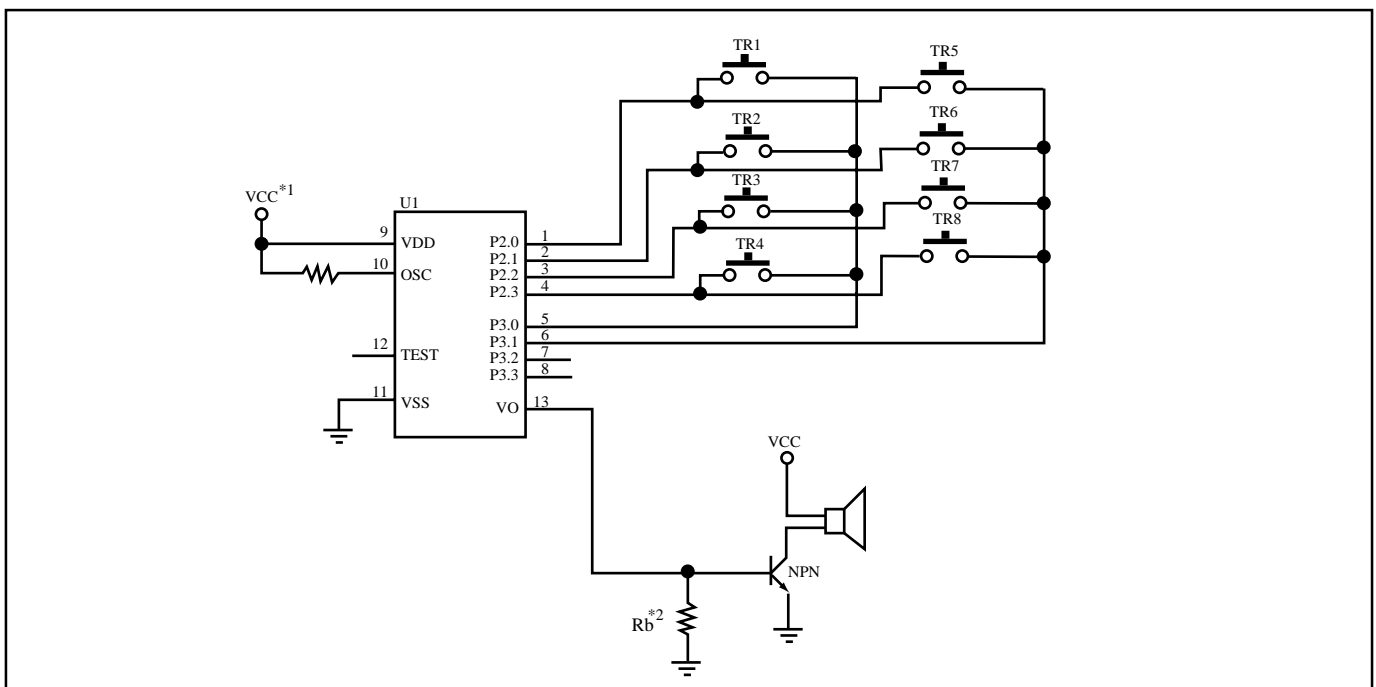
In the following application circuits:

- \*1 : For heavy loading application, adding an electrolytic capacitor between Vcc and Ground is recommended. The recommended value for button cell application is 10 $\mu$ F.
- \*2 : The recommended value for button cell application is 750 $\Omega$  or less.

### 4-key Application Circuit



### 8-key Application Circuit

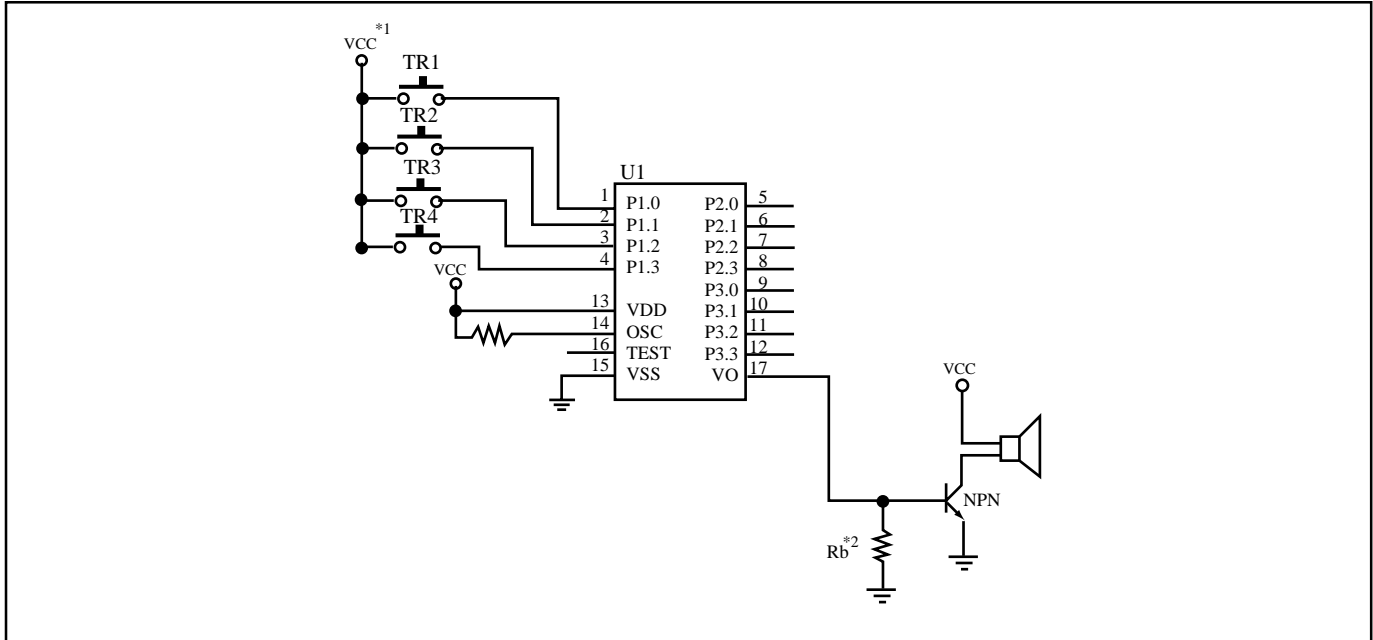


### APPLICATION CIRCUIT FOR EM57100 AND ABOVE

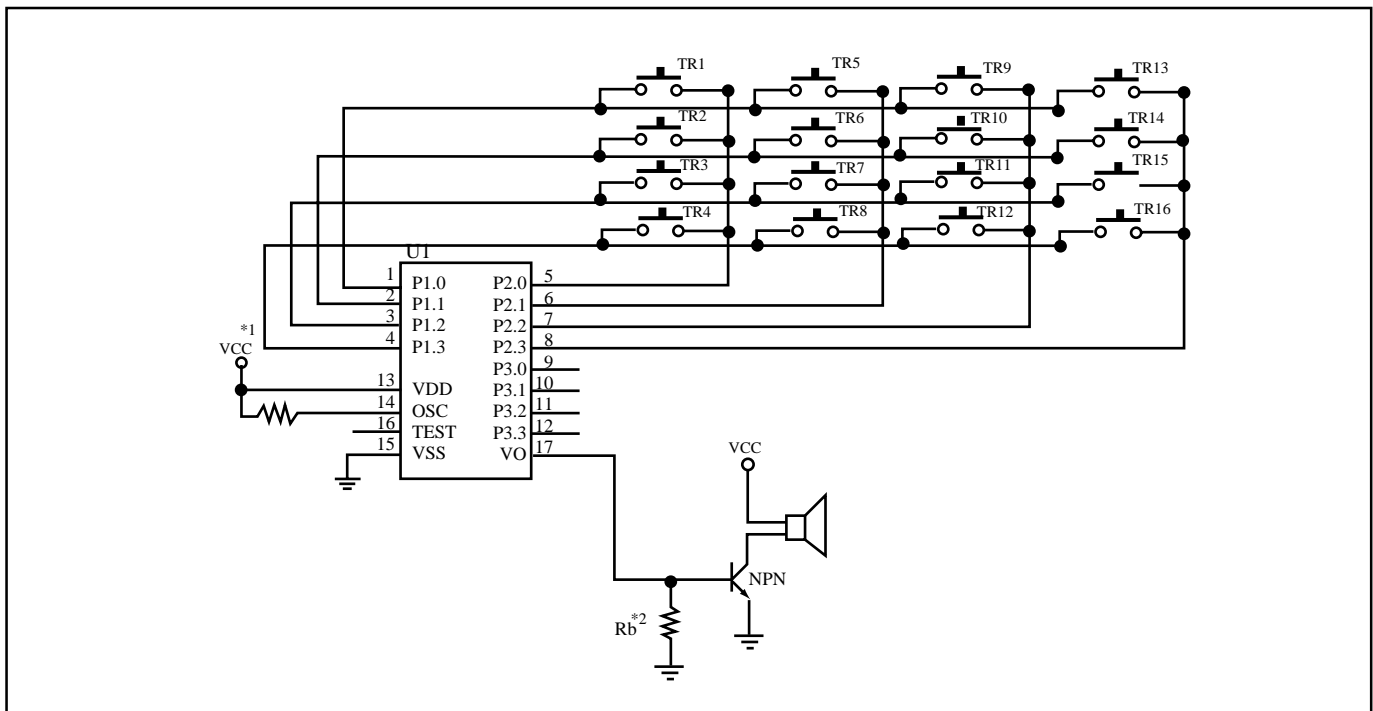
In the following application circuits:

- \*1 : For heavy loading application, adding an electrolytic capacitor between Vcc and Ground is recommended. The recommended value for button cell application is 10 $\mu$ F.
- \*2 : The recommended value for button cell application is 750 $\frac{1}{2}$  or less.

#### 4-key Application Circuit

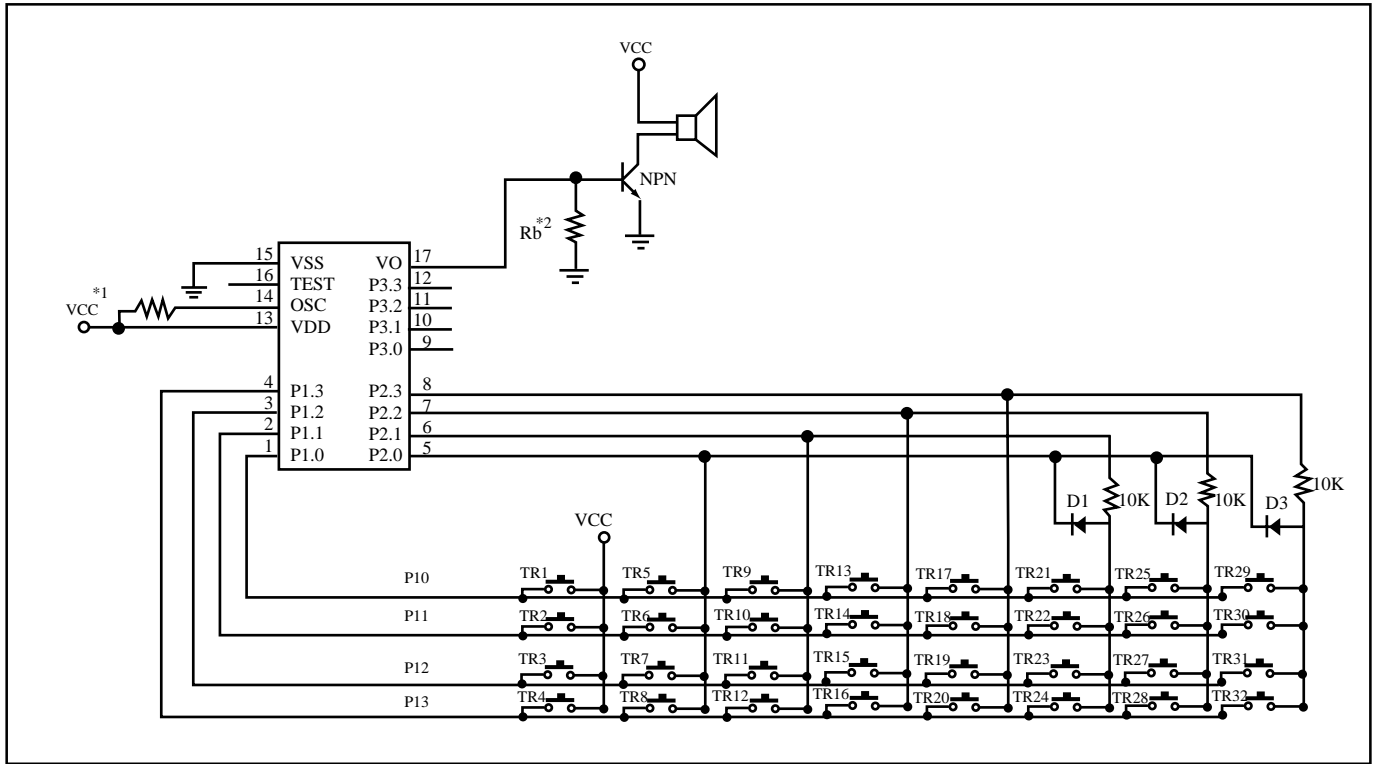


#### 16-key Application Circuit

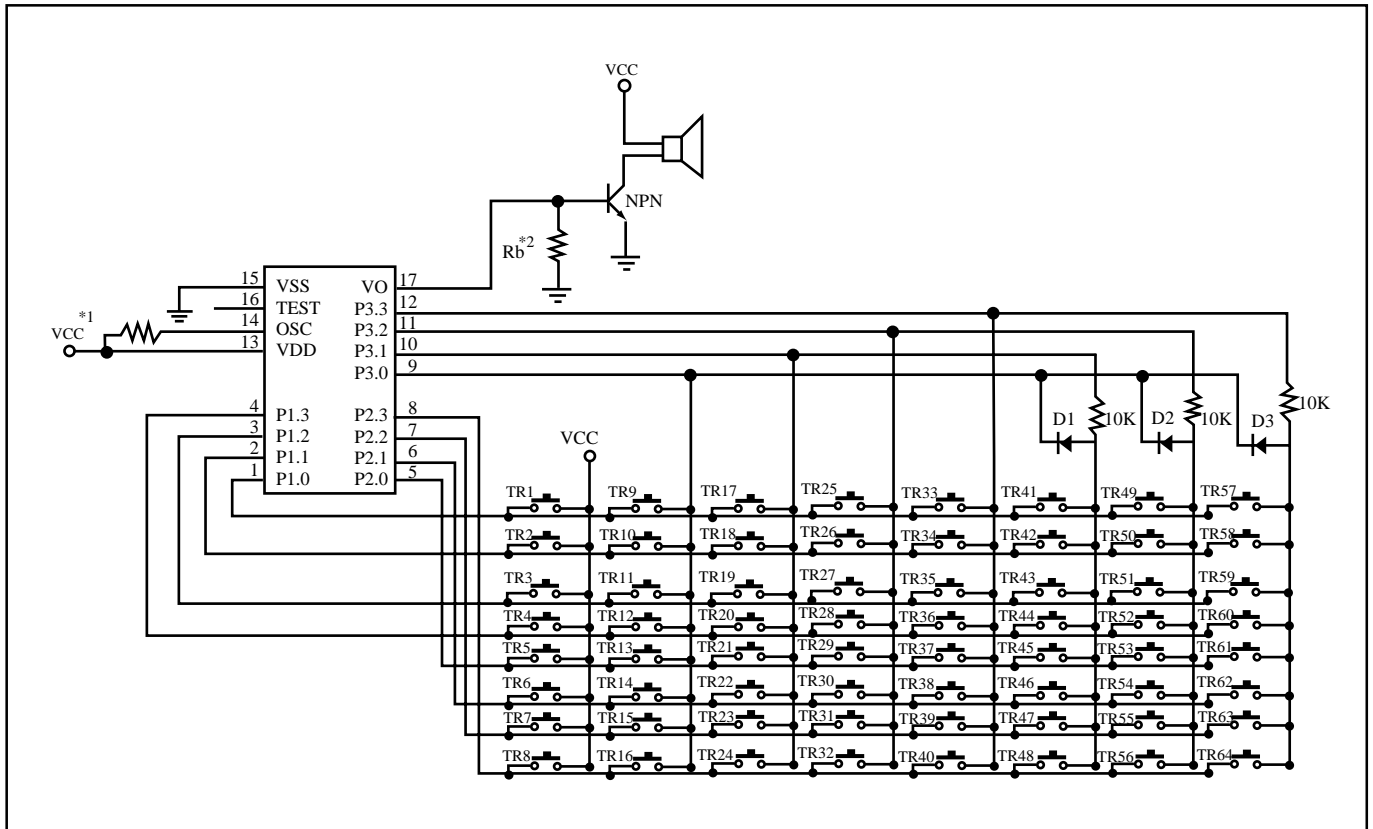


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32-key Application Circuit

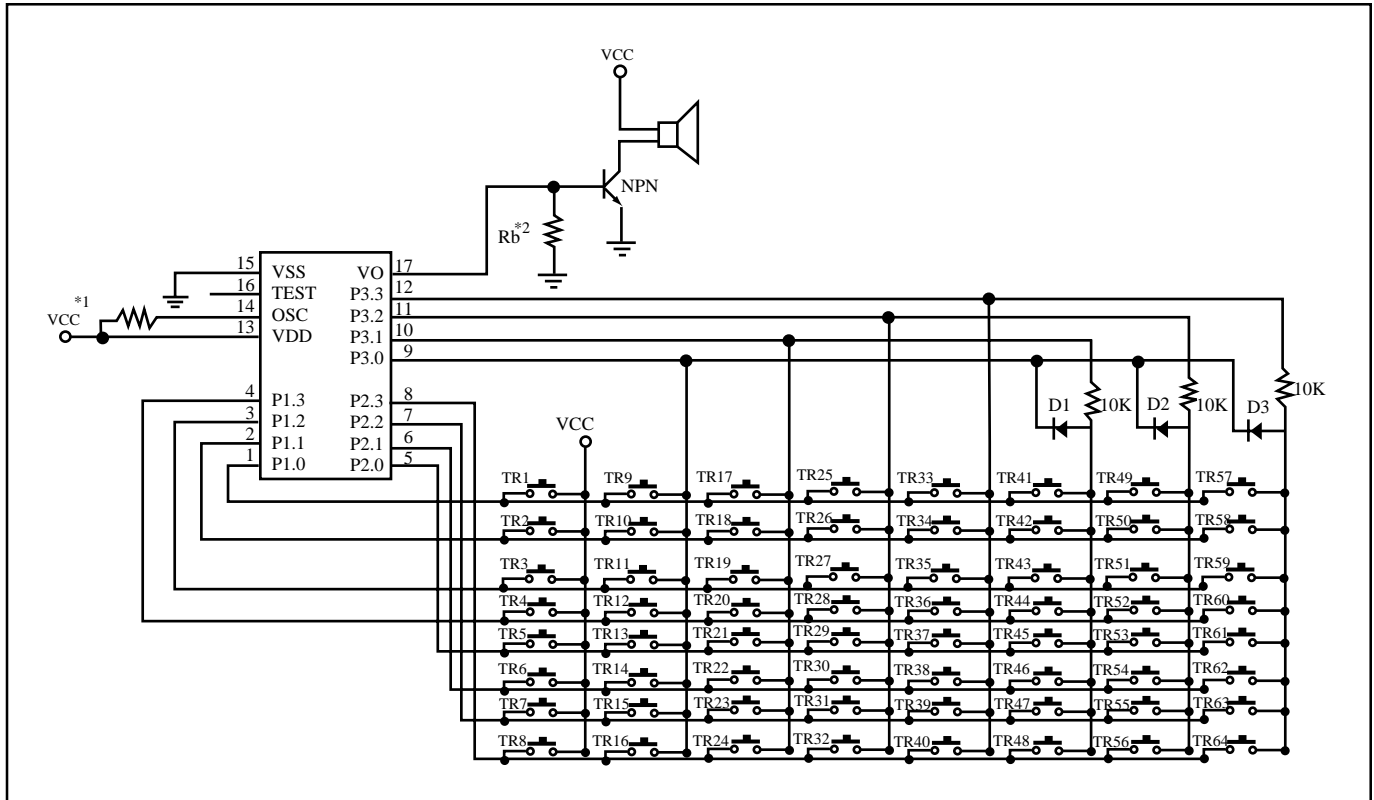


64-key Application Circuit

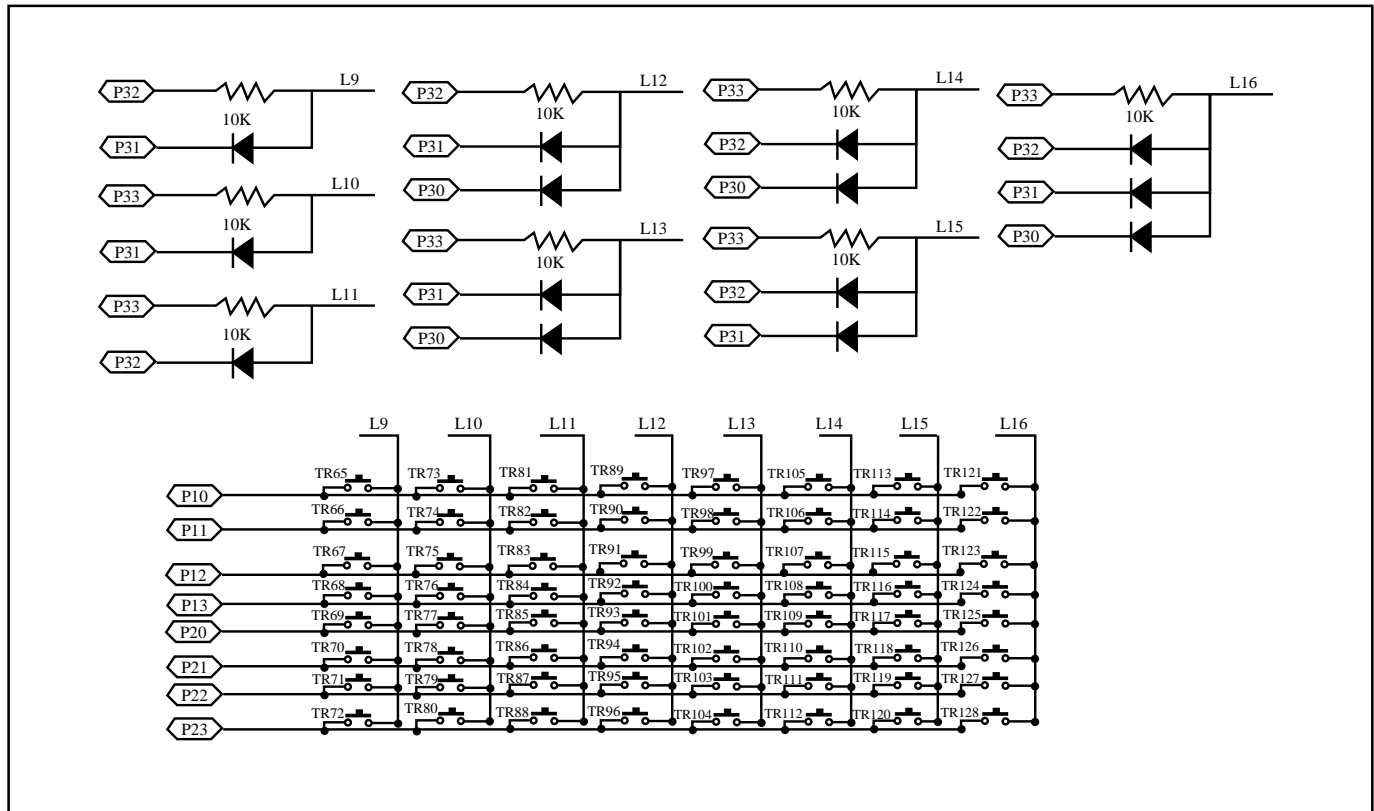


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128-key Application Circuit (A)

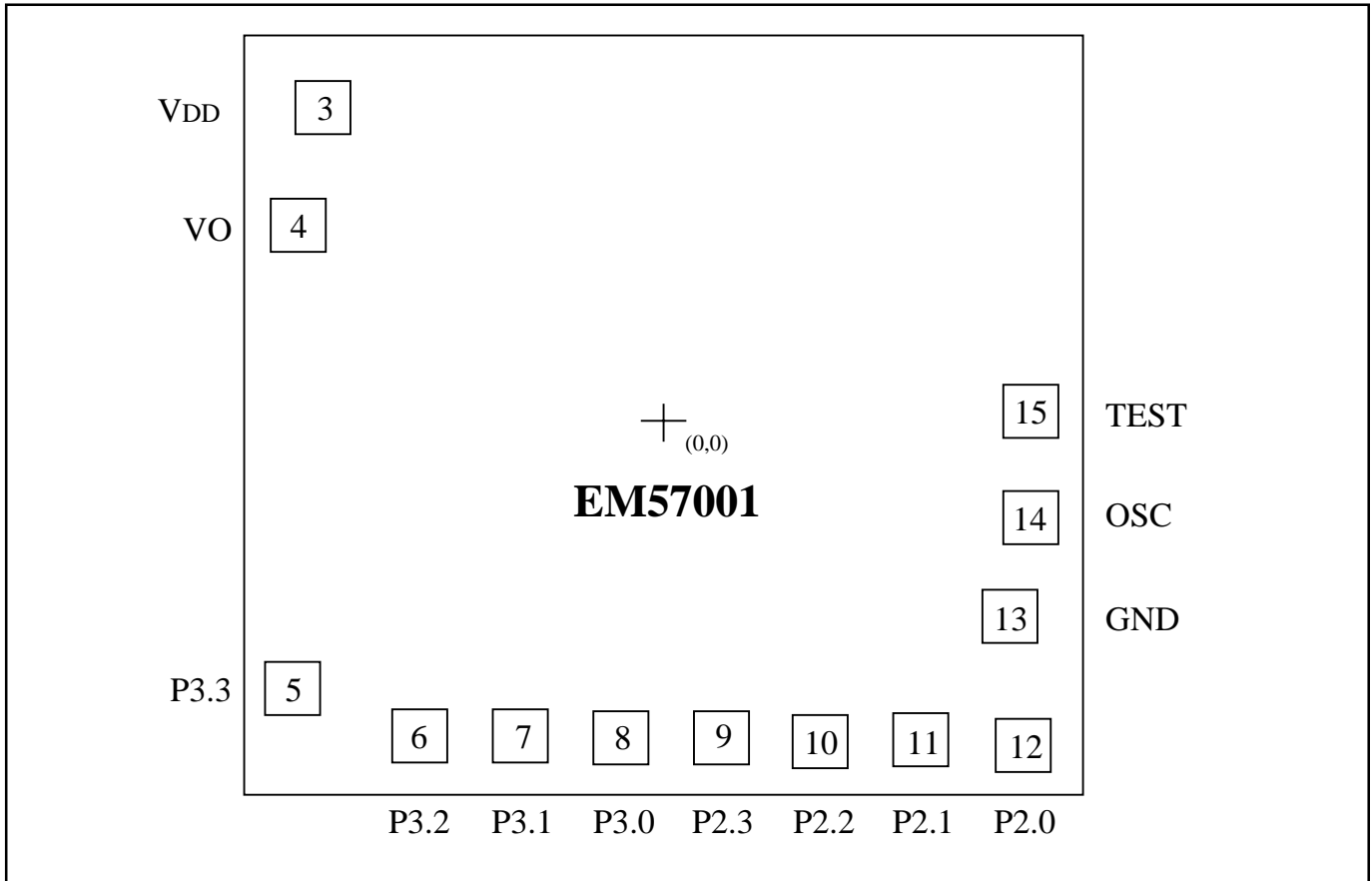


128-key Application Circuit (B)



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**PAD DIAGRAM**

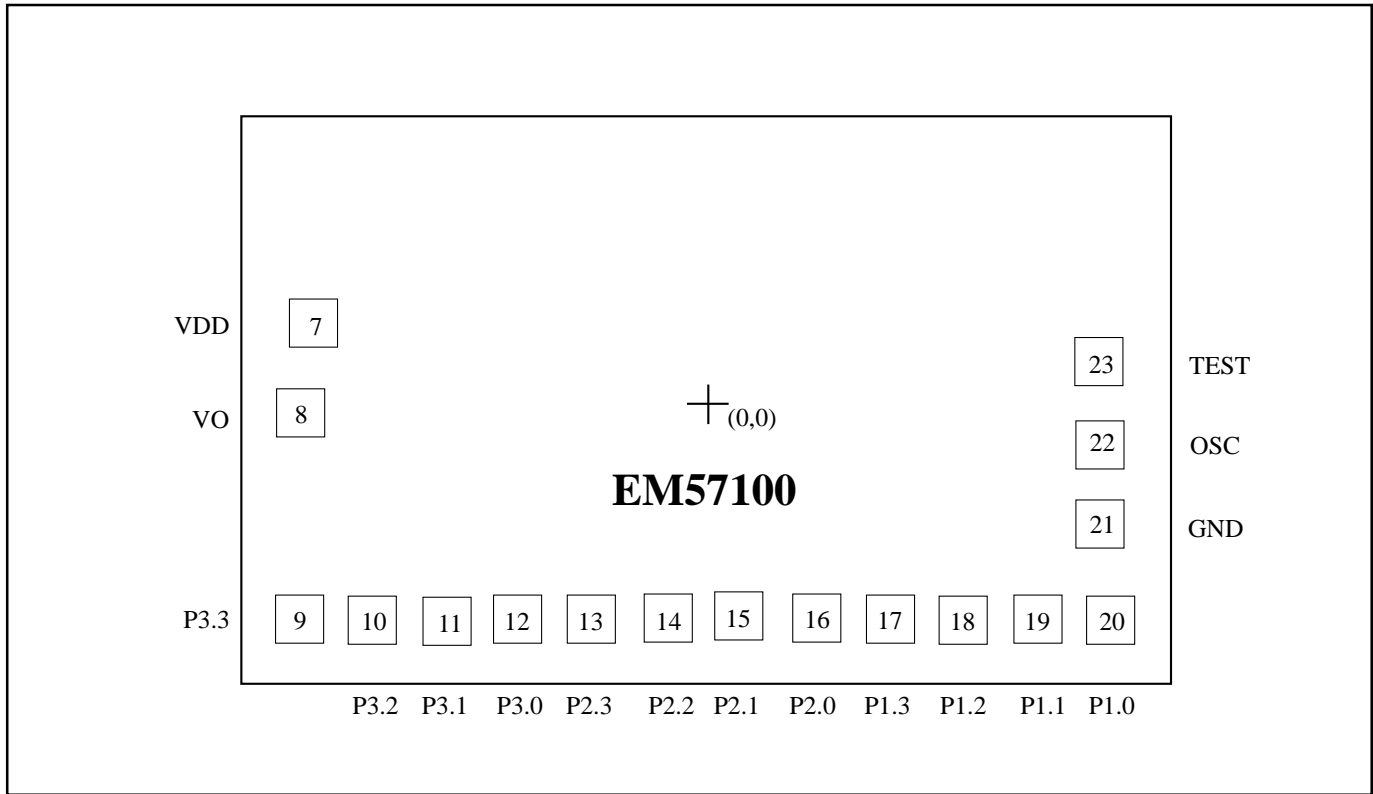


Chip Size : 1600um x 1400um

Note : For PCB layout, IC substrate must be connected to Vss.

Pad No.	Symbol	X	Y
3	VDD	-569.5	486.0
4	VO	-602.5	304.0
5	P3.3	-602.5	-463.4
6	P3.2	-437.0	-522.5
7	P3.1	-271.2	-522.5
8	P3.0	-105.6	-522.5
9	P2.3	60.2	-522.5
10	P2.2	225.7	-522.5
11	P2.1	391.5	-522.5
12	P2.0	557.1	-522.5
13	GND	580.2	-360.4
14	OSC	607.6	-40.4
15	TEST	607.6	130.7

**PAD DIAGRAM**



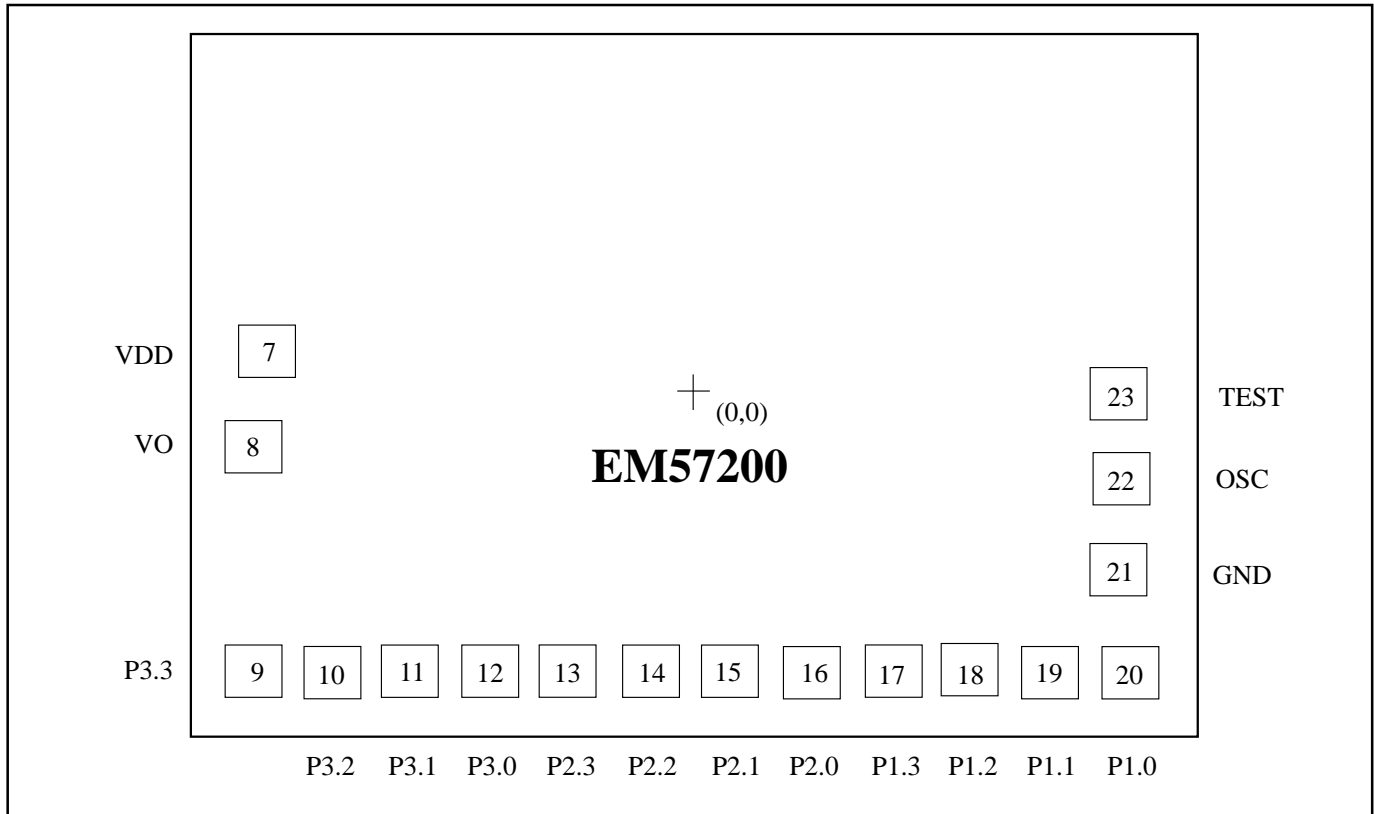
Chip Size : 1900um x 1200um

Note : For PCB layout, IC substrate must be connected to Vss.

Pad No.	Symbol	X	Y
7	VDD	-738.1	143.3
8	VO	-764.2	-22.4
9	P3.3	-764.2	-402.5
10	P3.2	-626.2	-402.5
11	P3.1	-491.4	-398.3
12	P3.0	-353.5	-398.3
13	P2.3	-217.9	-398.3
14	P2.2	-72.9	-398.3
15	P2.1	62.8	-398.3
16	P2.0	207.8	-398.3
17	P1.3	343.4	-399.7
18	P1.2	482.0	-399.7
19	P1.1	616.1	-399.7
20	P1.0	754.7	-399.7
21	GND	733.1	-222.0
22	OSC	737.2	-67.0
23	TEST	737.2	77.2



**PAD DIAGRAM**

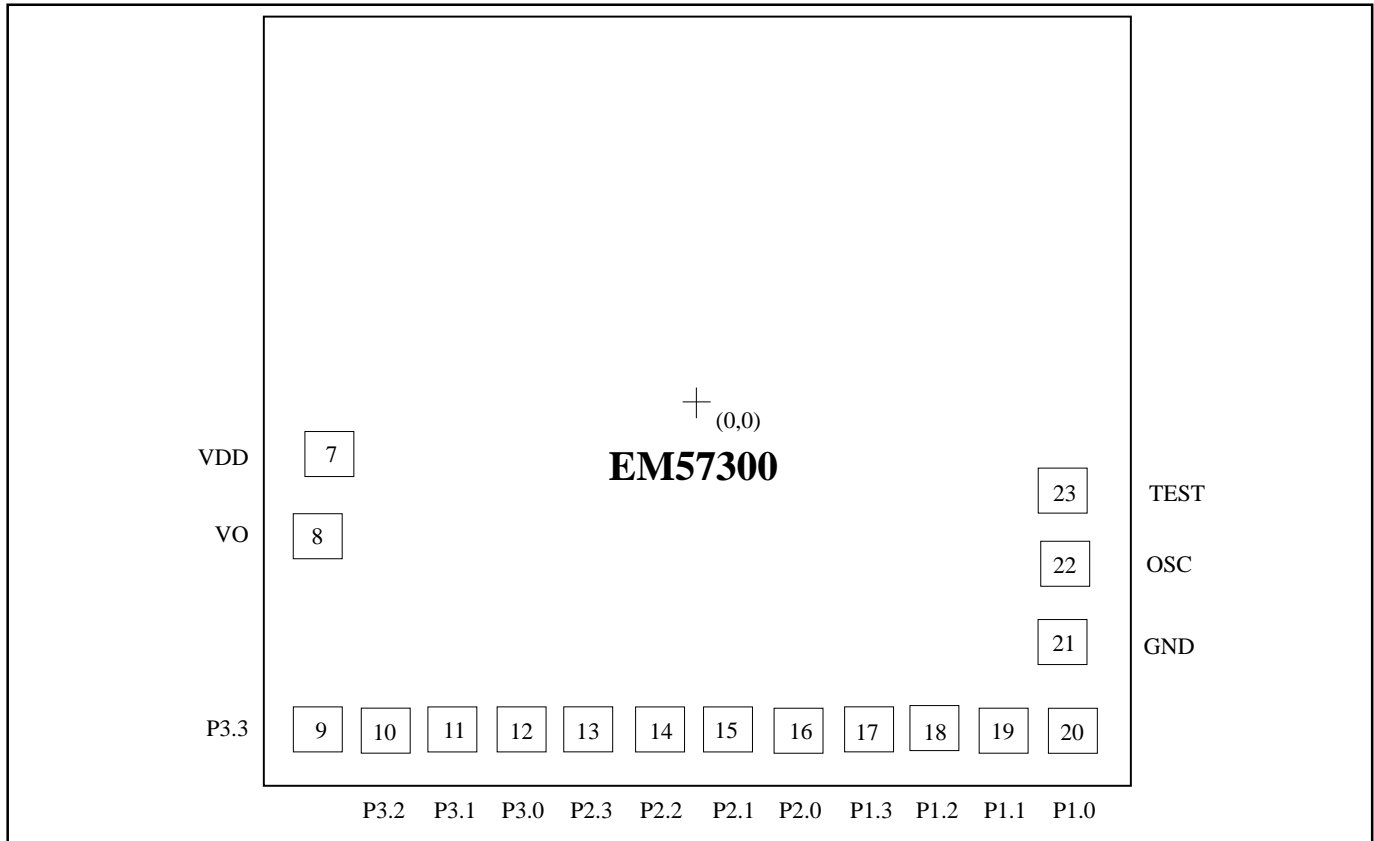


Chip Size : 1900um x 1400um

Note : For PCB layout, IC substrate must be connected to Vss.

Pad No.	Symbol	X	Y
7	VDD	-738.1	63.3
8	VO	-764.2	-102.4
9	P3.3	-764.2	-482.5
10	P3.2	-626.2	-482.5
11	P3.1	-491.4	-478.3
12	P3.0	-353.5	-478.3
13	P2.3	-217.9	-478.3
14	P2.2	-72.9	-478.3
15	P2.1	62.8	-478.3
16	P2.0	207.8	-478.3
17	P1.3	343.4	-479.7
18	P1.2	482.0	-479.7
19	P1.1	616.1	-479.7
20	P1.0	754.7	-479.7
21	GND	733.1	-302.0
22	OSC	737.2	-147.0
23	TEST	737.2	-2.8

**PAD DIAGRAM**

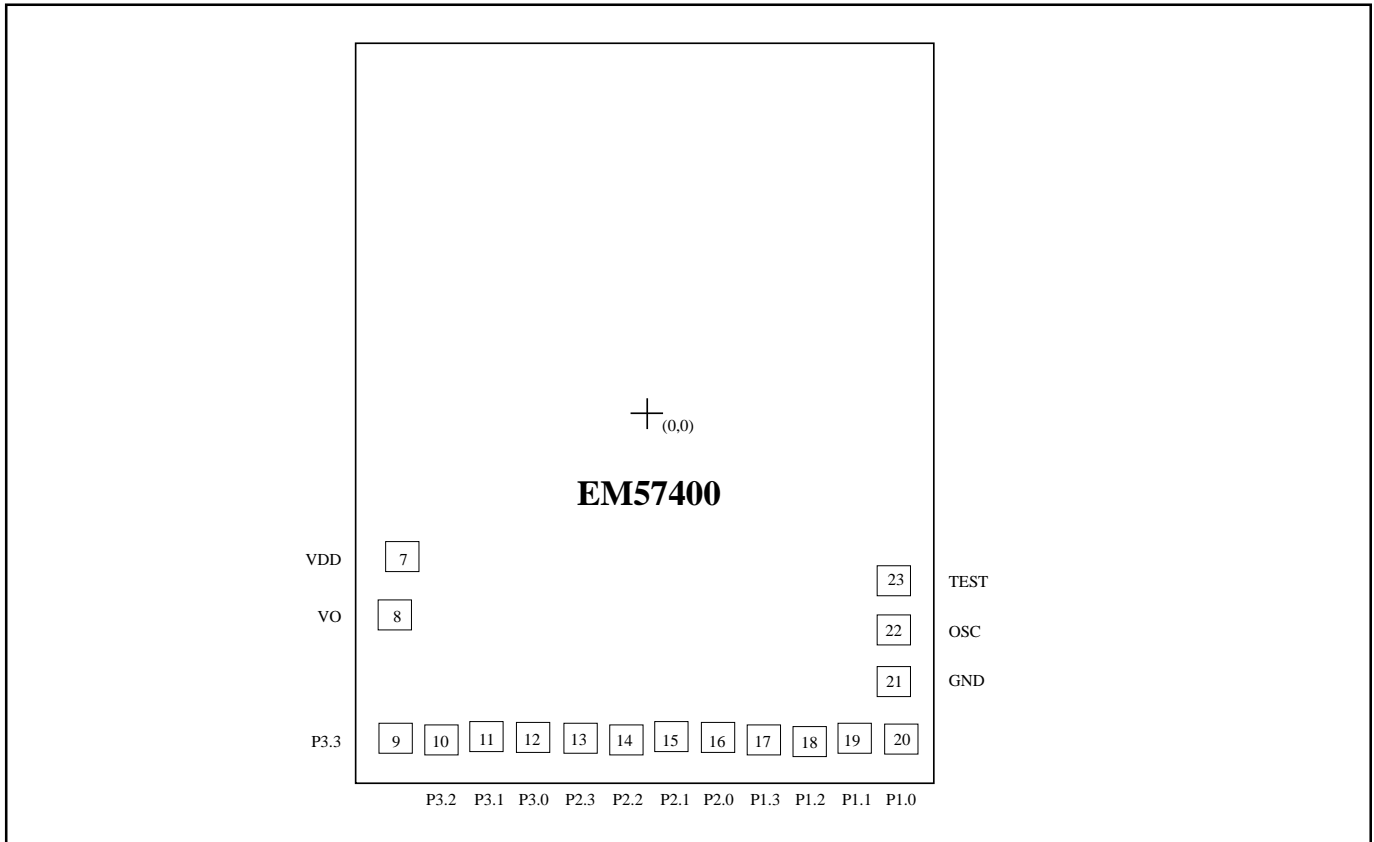


Chip Size : 1900um x 1700um

Note : For PCB layout, IC substrate must be connected to Vss.

Pad No.	Symbol	X	Y
7	VDD	-738.1	-101.7
8	VO	-764.2	-267.4
9	P3.3	-764.2	-647.5
10	P3.2	-626.2	-647.5
11	P3.1	-491.4	-643.3
12	P3.0	-353.5	-643.3
13	P2.3	-217.9	-643.3
14	P2.2	-72.9	-643.3
15	P2.1	62.8	-643.3
16	P2.0	207.8	-643.3
17	P1.3	343.4	-644.7
18	P1.2	482.0	-644.7
19	P1.1	616.1	-644.7
20	P1.0	754.7	-644.7
21	GND	733.1	-467.0
22	OSC	737.2	-312.0
23	TEST	737.2	-167.8

**PAD DIAGRAM**



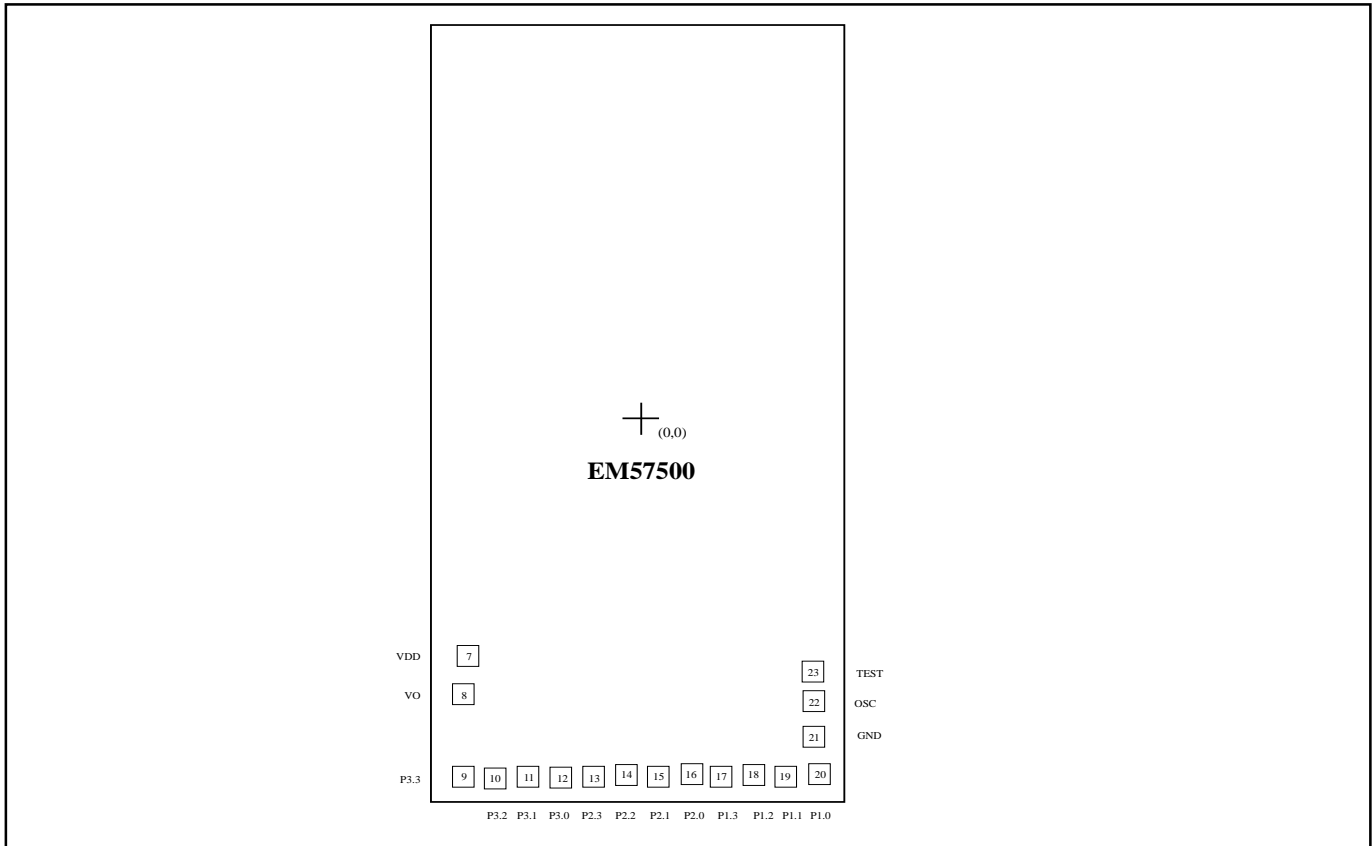
Chip Size : 1900um x 2400um

Note : For PCB layout, IC substrate must be connected to Vss.

Pad No.	Symbol	X	Y
7	VDD	-738.1	-426.7
8	VO	-764.2	-592.4
9	P3.3	-764.2	-972.5
10	P3.2	-626.2	-972.5
11	P3.1	-491.4	-968.3
12	P3.0	-353.5	-968.3
13	P2.3	-217.9	-968.3
14	P2.2	-72.9	-968.3
15	P2.1	62.8	-968.3
16	P2.0	207.8	-968.3
17	P1.3	343.4	-969.7
18	P1.2	482.0	-969.7
19	P1.1	616.1	-969.7
20	P1.0	754.7	-969.7
21	GND	733.1	-792.0
22	OSC	737.2	-637.0
23	TEST	737.2	-492.8

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**PAD DIAGRAM**



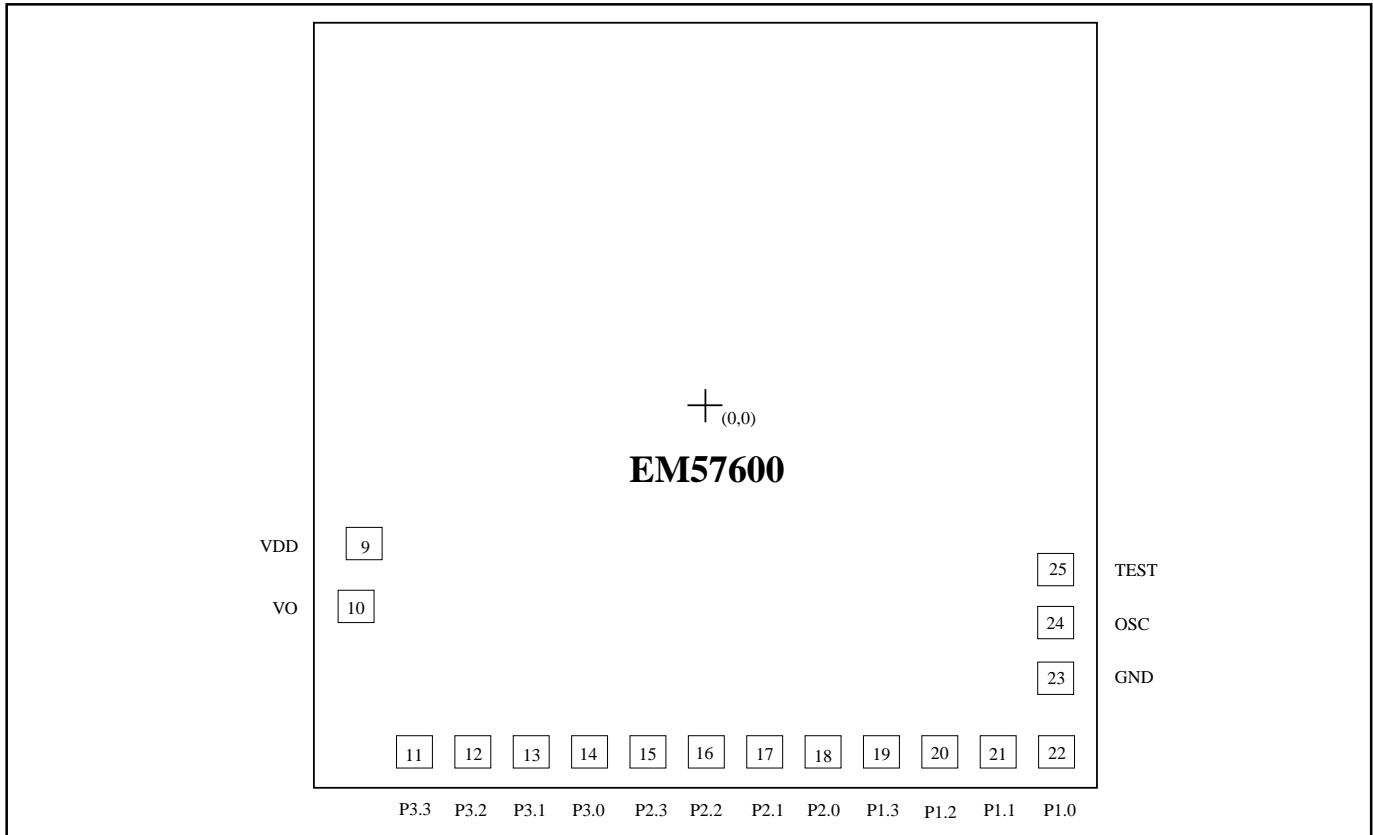
Chip Size : 1900um x 3700um

Note : For PCB layout, IC substrate must be connected to Vss.

Pad No.	Symbol	X	Y
7	VDD	-738.1	-1076.8
8	VO	-764.2	-1242.4
9	P3.3	-764.2	-1622.5
10	P3.2	-626.2	-1622.5
11	P3.1	-491.4	-1618.3
12	P3.0	-353.5	-1618.3
13	P2.3	-217.9	-1618.3
14	P2.2	-72.9	-1618.3
15	P2.1	62.8	-1618.3
16	P2.0	207.8	-1618.3
17	P1.3	343.4	-1619.7
18	P1.2	482.0	-1619.7
19	P1.1	616.1	-1619.7
20	P1.0	754.7	-1619.7
21	GND	733.1	-1442.0
22	OSC	737.2	-1287.0
23	TEST	737.2	-1142.8

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**PAD DIAGRAM ( XM/XP Version )**



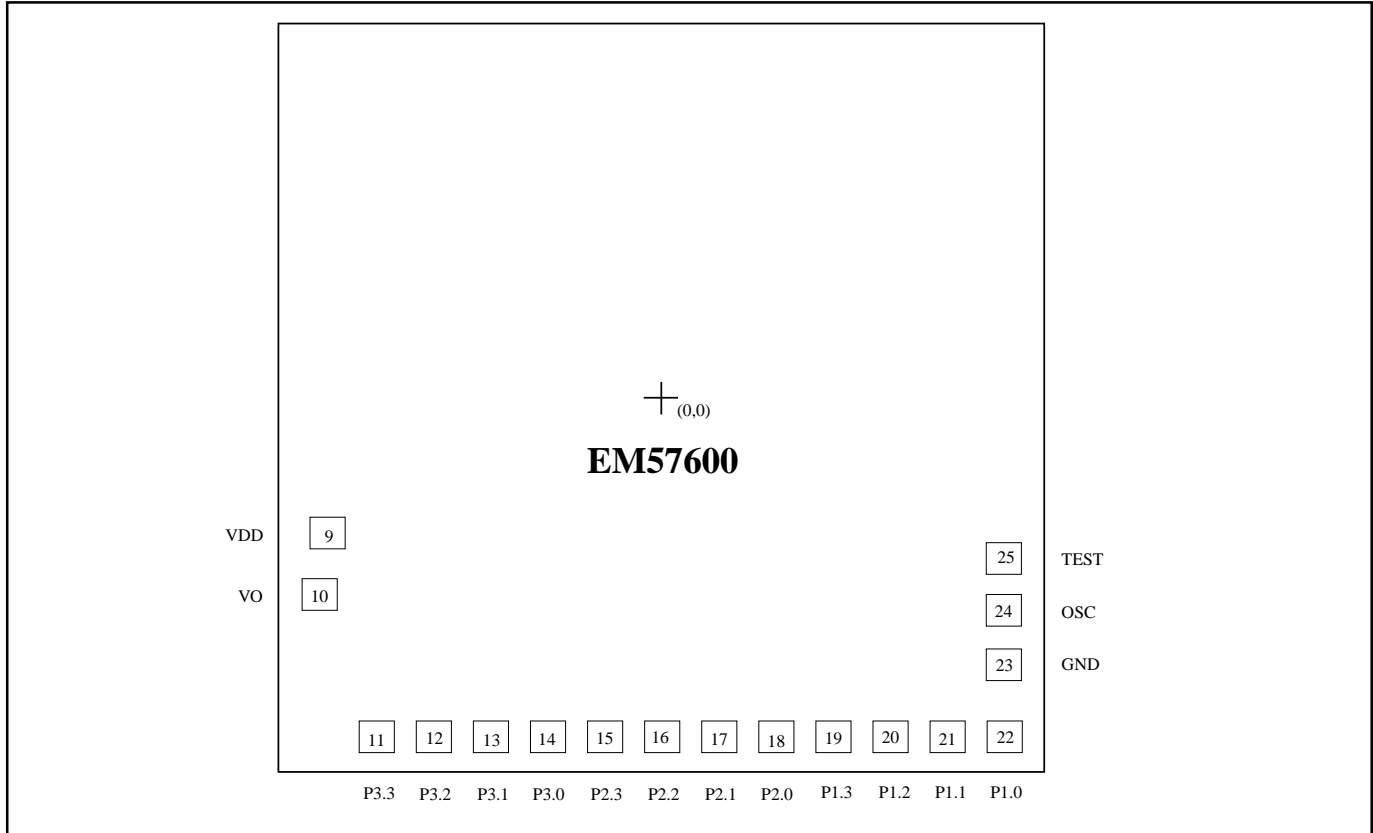
Chip Size : 3600um x 3800um

Note : For PCB layout, IC substrate must be connected to Vss.

Pad No.	Symbol	X	Y
9	VDD	-1538.1	-1060.2
10	VO	-1564.2	-1249.2
11	P3.3	-1266.3	-1670.8
12	P3.2	-1016.5	-1670.8
13	P3.1	-766.7	-1670.8
14	P3.0	-516.9	-1670.8
15	P2.3	-261.2	-1670.8
16	P2.2	0.0	-1670.8
17	P2.1	261.4	-1670.8
18	P2.0	522.6	-1670.8
19	P1.3	778.7	-1670.8
20	P1.2	1029.0	-1670.8
21	P1.1	1279.7	-1670.8
22	P1.0	1530.0	-1670.8
23	GND	1539.5	-1487.0
24	OSC	1543.4	-1332.0
25	TEST	1543.4	-1178.9

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**PAD DIAGRAM ( XR Version )**



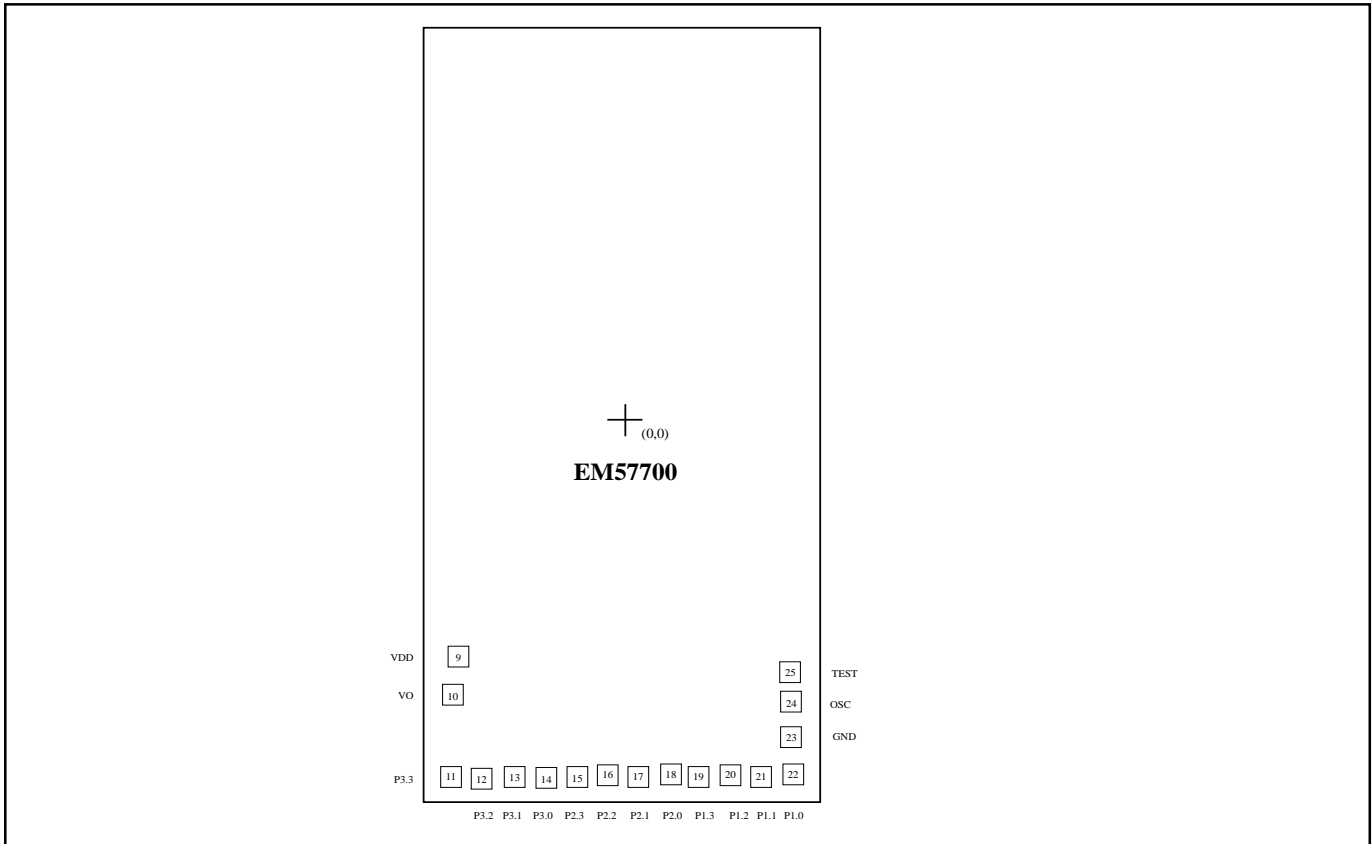
Chip Size : 3150um x 3200um

Note : For PCB layout, IC substrate must be connected to Vss.

Pad No.	Symbol	X	Y
9	VDD	-1372.7	-875.1
10	VO	-1368.5	-1074.8
11	P3.3	-1153.3	-1439.7
12	P3.2	-947.1	-1439.7
13	P3.1	-743.0	-1439.7
14	P3.0	-536.9	-1439.7
15	P2.3	-320.1	-1439.7
16	P2.2	-100.0	-1439.7
17	P2.1	129.5	-1439.7
18	P2.0	349.6	-1439.7
19	P1.3	574.1	-1439.7
20	P1.2	783.3	-1439.7
21	P1.1	1002.9	-1439.7
22	P1.0	1212.0	-1439.7
23	GND	1407.4	-1302.8
24	OSC	1403.4	-1138.2
25	TEST	1403.4	-962.3

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**PAD DIAGRAM**



Chip Size : 3600um x 6500um

Note : For PCB layout, IC substrate must be connected to Vss.

Pad No.	Symbol	X	Y
9	VDD	-1538.1	-2360.2
10	VO	-1564.2	-2549.3
11	P3.3	-1266.3	-2970.9
12	P3.2	-1016.5	-2970.9
13	P3.1	-766.7	-2970.9
14	P3.0	-516.9	-2970.9
15	P2.3	-261.2	-2970.9
16	P2.2	0.0	-2970.9
17	P2.1	261.4	-2970.9
18	P2.0	522.6	-2970.9
19	P1.3	778.7	-2970.9
20	P1.2	1029.0	-2970.9
21	P1.1	1279.7	-2970.9
22	P1.0	1530.0	-2970.9
23	GND	1539.5	-2787.0
24	OSC	1543.4	-2632.0
25	TEST	1543.4	-2478.9

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